

# SPORE: Combining Symmetry and Partial Order Reduction

MICHALIS KOKOLOGIANNAKIS, MPI-SWS, Germany

IASON MARMANIS, MPI-SWS, Germany

VIKTOR VAFEIADIS, MPI-SWS, Germany

Symmetry reduction (SR) and partial order reduction (POR) aim to scale up model checking by exploiting the underlying program structure: SR avoids exploring executions equivalent up to some permutation of symmetric threads, while POR avoids exploring executions equivalent up to reordering of independent instructions. While both SR and POR have been well studied individually, their combination in the context of stateless model checking has remained an open problem.

In this paper, we present SPORE, the first stateless model checker that combines SR and POR in a sound, complete and optimal manner. SPORE can leverage both symmetries in the client program itself, but also *internal symmetries* in the underlying implementation (i.e., idempotent operations), a novel symmetry notion we introduce in this paper. Our experiments confirm that SPORE explores drastically fewer executions than tools that solely employ SR/POR, thereby greatly advancing the state-of-the-art.

CCS Concepts: • **Theory of computation** → **Concurrency**; **Verification by model checking**.

Additional Key Words and Phrases: Model Checking, Dynamic Partial Order Reduction, Symmetry Reduction

## ACM Reference Format:

Michalis Kokologiannakis, Iason Marmanis, and Viktor Vafeiadis. 2024. SPORE: Combining Symmetry and Partial Order Reduction. *Proc. ACM Program. Lang.* 8, PLDI, Article 219 (June 2024), 58 pages. <https://doi.org/10.1145/3656449>

## 1 Introduction

Stateless model checking (SMC) [Godefroid 1997] verifies a concurrent program by enumerating all of its executions. SMC is quite popular in concurrent program verification as (a) can be used by programmers without any expertise in formal methods, (b) it can handle programs in full-fledged programming languages like C, C++ and Java, and (c) it can reason about the effects of the underlying weak memory model (e.g., C/C++11 [Lahav et al. 2017]). On the downside, however, SMC only supports verification of bounded programs, and often does not scale well enough to handle client programs with a sufficient number of threads to provide strong confidence the correctness of a given implementation.

There are two sound techniques that can be employed to increase the scalability of SMC.

*Symmetry reduction* (SR) [Clarke et al. 1996; Emerson and Wahl 2005] exploits symmetries in the threads of the program under test (e.g., all threads running the same code) and avoids to consider all the ways in which symmetric threads interleave, as the order in which such threads execute is

---

Authors' Contact Information: Michalis Kokologiannakis, MPI-SWS, Kaiserslautern, Germany, [michalis@mpi-sws.org](mailto:michalis@mpi-sws.org); Iason Marmanis, MPI-SWS, Kaiserslautern, Germany, [imarmanis@mpi-sws.org](mailto:imarmanis@mpi-sws.org); Viktor Vafeiadis, MPI-SWS, Kaiserslautern, Germany, [viktor@mpi-sws.org](mailto:viktor@mpi-sws.org).

---

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for third-party components of this work must be honored. For all other uses, contact the owner/author(s).

© 2024 Copyright held by the owner/author(s).

ACM 2475-1421/2024/6-ART219

<https://doi.org/10.1145/3656449>

clearly irrelevant. As an example of SR, consider the **FAIS** program where  $N$  symmetric threads perform an atomic “fetch-and-increment” operation on  $x$ :

$$\text{fetch\_add}(x, 1) \parallel \dots \parallel \text{fetch\_add}(x, 1) \quad (\text{FAIS})$$

While naive SMC explores  $N!$  executions for this program, SR only explores 1 execution.

*Dynamic partial order reduction* (DPOR) [Abdulla et al. 2014; Flanagan and Godefroid 2005] reduces the program state space by not exploring executions that are equivalent up to some permutation of independent instructions (e.g., instructions accessing different variables). For instance, consider the program below where 26 (non-symmetric) threads write different parts of an array:

$$a := 1 \parallel b := 2 \parallel \dots \parallel z := 26 \quad (\text{ARRAY})$$

For **ARRAY**, naive SMC would again explore  $26!$  executions while DPOR would only explore 1, as it notices that all threads access different parts of memory, and hence their relative order is irrelevant.

A common way to view both SR and DPOR is via the *equivalence partitioning* they induce on the program state space. Indeed, SR groups together executions that can be obtained from one another by changing the ID of symmetric threads, while DPOR groups together executions that can be obtained from one another by changing the order of non-conflicting instructions.

Observe, however, that even for symmetric programs, SR and DPOR are not equivalent, and neither approach subsumes the other. This can be seen with the example below:

$$\begin{array}{l} i := \text{fetch\_add}(x, 1) \\ a[i] := i \end{array} \parallel \dots \parallel \begin{array}{l} i := \text{fetch\_add}(x, 1) \\ a[i] := i \end{array} \quad (\text{FAIS+ARRAY})$$

While DPOR explores  $N!$  executions for **FAIS+ARRAY** (due to the conflicting `fetch_add`s), SR explores  $(2N - 1)!!$  executions (double factorial of odd numbers). This discrepancy is because in SMC, after each thread has executed its `fetch_add`, symmetry “breaks”, as each thread reads a different value.

Even though SR and DPOR are both effective when applied, existing SR/DROR approaches have two major limitations. First, they are incompatible: indeed, despite years of research on each of SR/DPOR, no algorithm manages to successfully combine the two, so employing one of them precludes the usage of the other. Second, both SR and DPOR fail to leverage *internal symmetries*, i.e., *idempotent* operations of the underlying implementation. One case of internal symmetry is the quintessential *helping* pattern, where some operation observes an ongoing operations of the same type that is incomplete, and then tries to complete the ongoing operation before performing its own. SR fails to exploit internal symmetries as the threads performing the operations are not sharing the same code, while DPOR fails to do so because the two operations are considered conflicting.

In this paper, we present **SPORE** (Symmetry and Partial Order Reduction Explorer), a novel algorithm that combines SR and DPOR, and overcomes both limitations above. **SPORE** resolves thread-level symmetries by restricting the coherence order of symmetric conflicting operations to agree with their thread order, and internal symmetries with a novel memory-model axiomatization that equates executions differing only in the order of the locally symmetric operations. The resulting algorithm is sound, complete and optimal under the combined equivalence partitionings, and achieves exponential reduction in verification time over the state-of-the-art. **SPORE** is also parametric in the choice of the underlying (weak) memory model.

Our contributions can be summarized as follows.

- §2 We (informally) describe why the combination of DPOR and SR is non-trivial, as well as how **SPORE** exploits thread-level and internal internal symmetries.
- §3 We present **SPORE** in detail and prove its correctness.
- §4 We implement **SPORE** in a tool for C/C++ programs, and empirically demonstrate that it is orders of magnitude faster than the state-of-the-art.

## 2 SPORE: Informal Description

We develop SPORE by adding SR on top of a DPOR algorithm (as opposed to the other way around), since DPOR underpins most modern SMC solutions [Abdulla et al. 2018; Aronis et al. 2018; Chalupa et al. 2017; Kokologiannakis et al. 2022, 2019b; Norris and Demsky 2013]. As such, we begin this section by explaining the basics of DPOR (§2.1), and then describe why the combination of DPOR and symmetry reduction is non-trivial and how SPORE achieves it (§2.2). We end the section by demonstrating how SPORE handles internal symmetries (§2.3).

### 2.1 Dynamic Partial Order Reduction

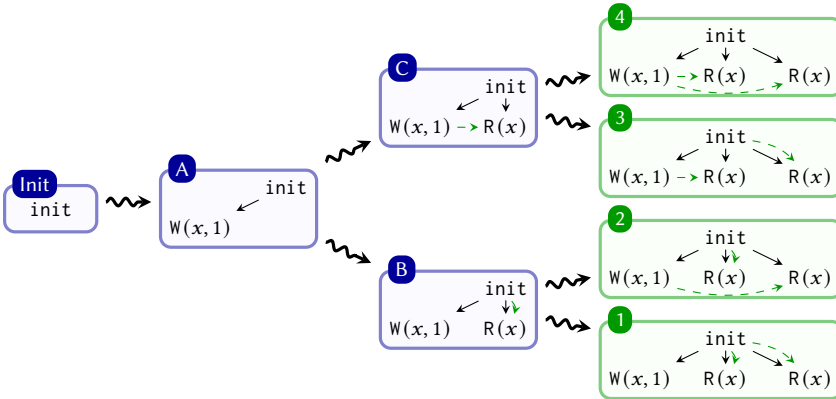
Modern DPOR algorithms, such as TRUST [Kokologiannakis et al. 2022], represent program executions up to the reordering of independent accesses in a structure called *execution graph* [Alglave et al. 2014], and verify a given program by constructing its associated execution graphs in an incremental fashion.

Each execution graph  $G$  comprises: (a) a set of events  $E$  (graph nodes), modeling instructions of the program, and (b) a few relations on events (graph edges), modeling various interactions between the instructions. In the following, we consider three such directed edges: the *program order* ( $po$ ), which orders instructions of the same thread, the *reads-from* relation ( $rf$ ), which relates each read event  $r$  in  $G$  to a write event  $w$  in  $G$ , from which  $r$  obtains its value, and the *coherence order* ( $co$ ), which totally orders writes at each memory location.

**Example 1** Consider the  $w+r+r$  program below.

$$T_1: x := 1 \parallel T_2: r_2 := x \parallel T_3: r_3 := x \quad (w+r+r)$$

Under sequential consistency (SC) [Lamport 1979], the program has four executions, 1–4, which model the four equivalence classes into which the  $3! = 6$  thread interleavings are partitioned. These graphs can be produced by the following DPOR exploration starting from the initial graph **Init** through the intermediate graphs **A**, **B**, and **C**.



The exploration proceeds in a depth-first manner: DPOR adds the events of the program from left to right, one by one, and whenever a read has more than one place to read from, DPOR initiates a recursive subexploration. For instance, when the read of  $T_2$  is added, it can read both 0 and 1 (both options are consistent according to SC), and thus DPOR initiates subexplorations **B** and **C**. DPOR proceeds in a similar manner, until all events of the program have been added to the graph.

### Conventions

Following standard conventions in the weak memory model literature, we (1) treat  $rf$  as a relation from the write to the read event; (2) assume a special initialization event  $init$ , which initializes every location with 0 and is thus  $po$ -before all other events and  $co$ -before all other write events; (3) we do not draw  $co$  edges from  $init$  to other writes (as it is trivially  $co$ -before them). In explorations, we use **letters** to refer to intermediate executions, **numbers** to refer to full executions, and **red** to denote executions that will not be explored.

*Revisits.* The exploration in Example 1 was largely straightforward, but there is still one aspect of DPOR we have not discussed: *revisiting*. For exposition purposes, suppose we add the events of  $w+r+r$  from right to left. When we encounter the reads, they cannot yet read 1 because the corresponding write does not exist in the graph. Therefore, whenever a write is added to a graph, DPOR also revisits existing same-location reads to see if they can read from the newly added write.

Whenever DPOR revisits a read  $r$  from a write  $w$ , it *restricts* the graph to remove some of the events added to the graph after  $r$ , since they may depend on the value read by  $r$ . (If not, they will be re-added in subsequent steps of the exploration.) The most common choice for restricting the graph is to keep only the events that were added before  $r$  and those causally before  $w$  (i.e., in its  $porf \triangleq (po \cup rf)^+$  prefix). For instance, in the right-to-left exploration of  $w+r+r$ , if  $W(x, 1)$  revisits the read of  $T_3$ , the resulting graph does not have the read of  $T_2$  because it was added after  $T_3$  and is not  $porf$ -before  $W(x, 1)$ .

The restriction due to revisits may lead to duplicate explorations, as we demonstrate below.

**Example 2** Consider the following variation of  $w+r+r$ .

$$T_1: x := 1 \parallel T_2: r_2 := x \parallel T_3: x := 2 \quad (w+r+w)$$

Adding the events from left to right, observe that there are two subexplorations where  $W(x, 2)$  has the chance to revisit the read of  $T_2$ : when the latter reads 0 and when it reads 1. These subexplorations are shown in Fig. 1. If  $W(x, 2)$  performs the revisit in both, the exact same graph will be created.



Fig. 1. Revisit opportunities

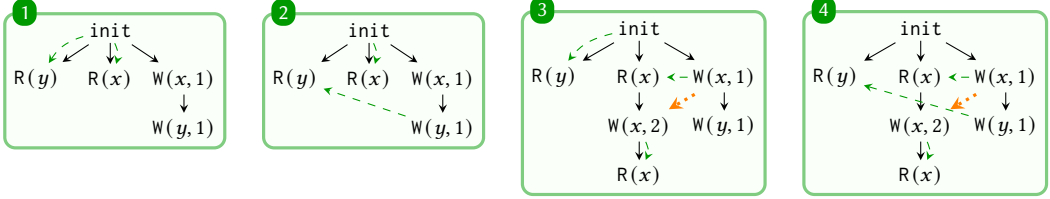
There are two ways DPOR can avoid such duplication. Abdulla et al. [2014] and Kokologiannakis et al. [2019b] simply save all encountered executions (more precisely: the ones created by revisits), and drop subsequent revisits that yield an already encountered execution. Storing executions, however, leads to exponential memory consumption in the size of the program under test.

*Avoiding Duplication with Maximal Extensions.* A better solution adopted by TRuST [Kokologiannakis et al. 2022] is to impose a *revisiting condition* so that a given revisit only takes place once among all possible subexplorations. The key observation is that whenever DPOR encounters two graphs that will yield the same graph immediately after a revisit, then in both cases the revisit happens from the same write  $w$  to the same read  $r$ , and the graphs only differ in the sets of events that were affected by the revisit (namely,  $r$  itself and all the events deleted by the revisit).

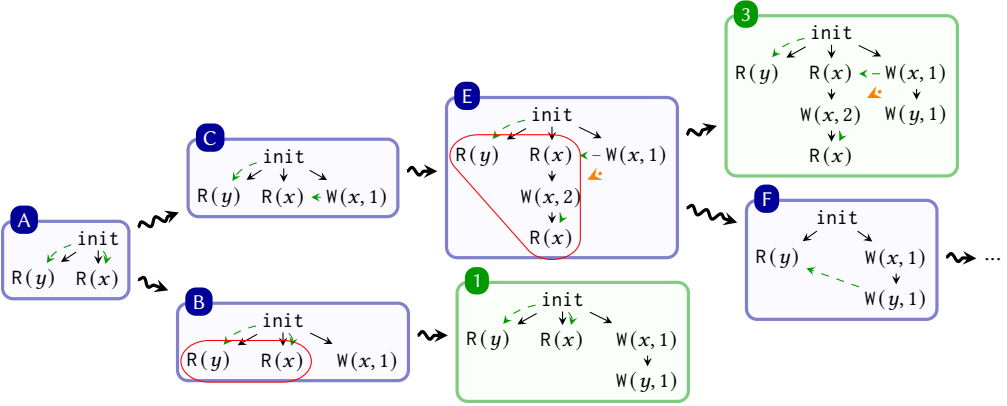
TRuST therefore constrains the events affected by the revisit (i.e., the read being revisited and the deleted events) to form a *maximal extension*: to be added  $co$ -maximally w.r.t. to the  $porf$ -prefix of the revisiting write. Maximal conditions are better understood with an example.

**Example 3** Consider the **REV-EX** below along with its SC-consistent execution graphs.

$$T_1: a := y \quad \parallel \quad T_2: \mathbf{if} (x = 1) \quad \parallel \quad T_3: x := 1 \\ x := 2 \quad \parallel \quad y := 1 \\ c := x \quad \parallel \quad$$
(REV-EX)



A DPOR run producing these execution can be seen below.



Assuming that DPOR adds events in a left-to-right manner, after adding the events of the first two threads, it then adds  $W(x, 1)$  which can either revisit  $R(x)$  or not (graphs **C** and **B**, respectively).

Following the respective subexplorations,  $W(y, 1)$  is encountered in both cases: in exploration **B** immediately, and in exploration **C** after adding the events under the conditional of  $T_2^1$ . Similarly to  $W(x, 1)$ , in both subexplorations,  $W(y, 1)$  has the opportunity to either revisit  $R(y)$  or not.

Revisiting  $R(y)$  in both cases, however, leads to duplication, as the same graph (graph **F**) will be obtained twice. Maximal extensions dictate that the revisit only takes place from execution **E**, as all the affected events are added maximally w.r.t.  $W(y, 1)$ . To see why, it is helpful to think ‘‘backwards’’: starting from the graph obtained from the revisit without the write and read participating in the revisit ( $W(y, 1)$  and  $R(y)$ ), if all the **affected** events are added in a **co-maximal** manner (i.e., reads reading the **co-latest** write and writes added last in **co**), we get graph **E**, which is the graph from where the revisit takes place.

To define maximal extensions, we first introduce an auxiliary definition about execution graphs. A write event  $w$  is **co-maximal** in a set of events  $E$  if  $w \in E$  and it does not have a **co**-successor in  $E$  (i.e.,  $\nexists w' \in E. \langle w, w' \rangle \in \mathbf{co}$ ).

<sup>1</sup>These events have a unique **co** and **rf** option as SC enforces coherence: informally,  $T_2$  is already aware of  $W(x, 1)$  so  $W(x, 2)$  has to be **co**-after it, and  $R(x)$  has to read the latest value  $T_2$  is aware of.

*Definition 2.1.* An event  $e$  in a graph  $G$  is *added maximally* w.r.t. a write event  $w$  in  $G$ , if the following conditions hold, where  $E$  is the set of all events  $e'$  added before  $e$  or in  $w$ 's `porf` prefix (i.e.,  $\langle e', w \rangle \in \text{porf}$ ):

- If  $e \in W$ , then  $e$  is `co`-maximal in  $E$ .
- If  $e \in R$ , then  $G.\text{rf}(e)$  is `co`-maximal in  $E$ .

Observe that non-write/read events are always added maximally w.r.t. a revisiting write.

Maximal extensions also have the following useful property, which we will use in some of our examples below.

**PROPOSITION 2.2.** *If a write  $w$  revisits a read  $r$  resulting in a graph  $G$ , the `porf`-prefix of  $w$  will not be removed in any of the subsequent subexplorations starting from  $G$  [Kokologiannakis et al. 2022].*

## 2.2 SPORE: Thread-Level Symmetries

Consider again the `W+R+R` example where  $T_2$  and  $T_3$  share their code.

$$T_1: x := 1 \parallel T_2: r_2 := x \parallel T_3: r_3 := x \quad (\text{W+R+R})$$

We say that executions **2** and **3** from its consistent executions (see Example 1) are symmetric because one can be obtained by permuting the symmetric threads of the other.

**2.2.1 Distinguishing Among Symmetric Executions.** To avoid exploring both graphs, we pick a *representative* execution among them and instrument DPOR to drop non-representative symmetric executions.

SPORE achieves this using thread IDs: we deem as representative the graph where a symmetric thread only reads values that are at least as “recent” (in terms of `co`) as the ones read by its symmetric predecessor. In the `W+R+R` example, this means that graph **2** is the representative one, as in graph **3** the read of  $T_2$  reads a value that is `co`-after the one read by  $T_3$ <sup>2</sup>.

Let us formalize this intuition. We say that two events  $e, e'$  in an execution graph  $G$  are *prefix-matching* (and write `prefix-matching`( $e, e'$ )), if they originate from threads with the same code and have matching `po`-prefixes, i.e., all events `po`-before them are either not memory accesses or reads that pairwise read from the same write. Note that two writes can be prefix-matching, but any `po`-later pair of events cannot be: writes break matching prefixes because they are `co`-ordered.

SPORE picks as representative graphs the ones where the thread order of prefix-matching events does not contradict an extension of `co` called *extended coherence order*:  $\text{eco} \triangleq (\text{co} \cup \text{rf} \cup \text{rb})^+$ , where  $\text{rb} \triangleq \text{rf}^{-1}$ ; `co` is the *reads-before* order, denoting that a read reads from a write whose value is later overwritten. Observe that, due to the definition of prefix-matching events above, any `eco` path between two prefix-matching events will involve `co`.

Given this notion of representative graphs, in the `W+R+W` example above, graph **2** in Example 1 is the representative because `eco` agrees with the thread order (there is an `rb`; `rf` path from  $T_2$  to  $T_3$ ), but graph **3** is not as `eco` contradicts the thread order.

**2.2.2 Problem #1: The Interaction Between Representative and Maximal Executions.** This solution, however, does not work that easily due to *revisiting* (§2.1). The problem is that SR avoids exploring certain graphs (i.e., the non-representative ones), the exploration of which DPOR might *require* so that a given revisit happens. Put differently, maximal extensions can be non-representative graphs.

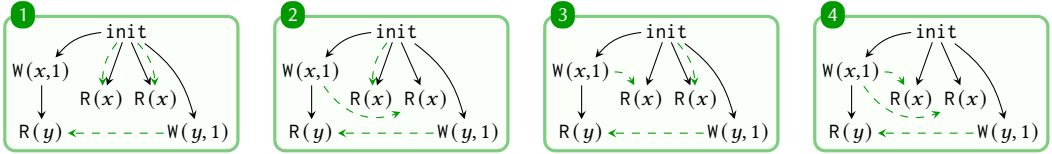
<sup>2</sup>Recall that all writes are `co`-after the initializer event.

**Example 4** To illustrate the problem, consider the following variation of **w+r+r** (again, T<sub>2</sub> and T<sub>3</sub> share their code), and suppose we are interested in the executions where  $a = 1$ .

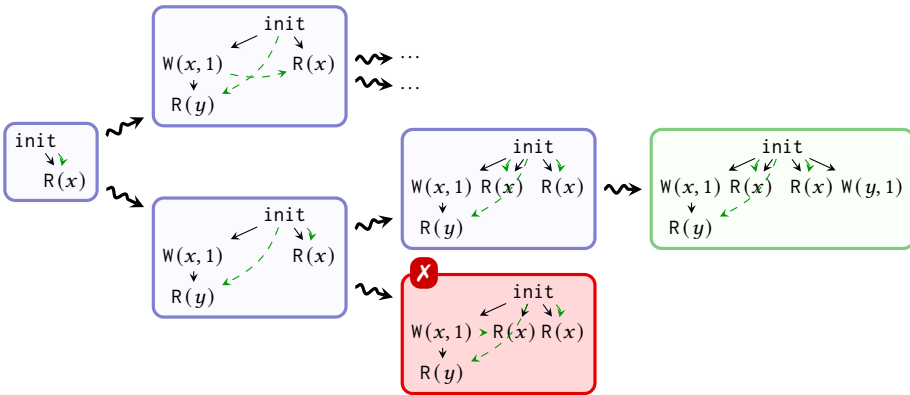
$$T_1: x := 1 \parallel T_2: r_2 := x \parallel T_3: r_3 := x \parallel T_4: y := 1 \quad (W+R+R-REV)$$

$$a := y$$

Similarly to **w+r+r**, graphs 2 and 3 are symmetric, and graph 2 is the representative one.



We now present a (partial) DPOR exploration of this program, with the objective of showing that the combination of DPOR and SR is not guaranteed to be correct. Concretely, we will show that execution 1 will not be generated if DPOR explores the program threads in a peculiar order<sup>3</sup>.



Suppose DPOR first adds the read of T<sub>3</sub>, and then proceeds with the events of T<sub>1</sub>. When it adds  $W(x, 1)$ , it can either revisit  $R(x)$  (top exploration tree) or not (bottom exploration tree). Since we are interested in generating execution 1, let us disregard the top exploration tree (where T<sub>3</sub> reads 1) and focus on the bottom one. (The reason we discard the top one is that DPOR does not “undo” revisits: since  $W(x, 1)$  revisits  $R(x)$  of T<sub>3</sub>, in all subsequent subexplorations T<sub>3</sub> keep reading 1; see Prop. 2.2.)

At the next step, the algorithm will add the read of T<sub>2</sub>, which can either read 1 (from T<sub>1</sub>) or 0 (the initial value). DPOR, however, will only consider the exploration where the read is reading 0, and not the execution where it reads 1, as the latter is not the representative among the symmetric ones. (The one where T<sub>2</sub> reads 0 and T<sub>3</sub> reads 1 is.)

At the final step, the algorithm will add the  $W(y, 1)$  event of T<sub>4</sub>, and will consider to revisit the  $R(y)$ . With the maximal extension condition of §2.1, however, this revisit is doomed to fail, since the read of T<sub>2</sub> is not added **co**-maximally w.r.t.  $W(y, 1)$ . Hence DPOR will not generate execution 1.

<sup>3</sup>DPOR should be able to generate all executions of a program irrespective of the order in which it encounters its threads.

As the **W+R+R-REV** example demonstrated, the problem when combining DPOR and SR is that resulting algorithm might deem the graphs on which TRUST's maximal extension condition enables a certain revisit as non-representative (and therefore drop them).

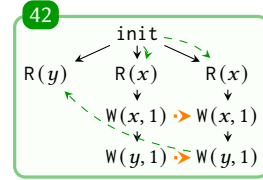
There are two potential solutions to this problem.

The first is to modify the maximal extension condition to hold only for representative graphs. Unfortunately, this approach does not work because of the atomicity condition of read-modify-write (RMW) operations. In our technical appendix [Kokologiannakis et al. 2024b], we show that it is impossible to define a maximality condition purely at the level of execution graphs without consulting the program.

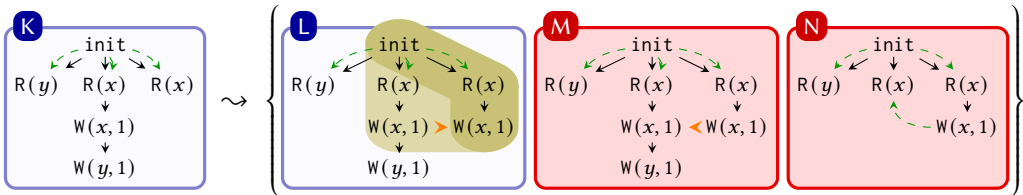
The second solution is to *keep* the maximal extension condition intact, but restrict the *exploration order* so that representative executions always form maximal extensions. To see why restricting the exploration order is a promising solution, let us consider again Example 4. The reason why a maximal extension was created in a non-representative execution was that T<sub>3</sub> was added before T<sub>2</sub> (i.e., against thread order), and T<sub>2</sub> had **co**-later options available to it (T<sub>1</sub> was added after T<sub>3</sub> but before T<sub>2</sub>). By fixing the exploration order, we essentially try to “force” **co** to agree with the thread order.

**2.2.3 Problem #2: Fixing the Exploration Order is Inadequate.** Given the above, a natural choice is to maintain a left-to-right scheduling among threads that share their code. Even though this simple modification mitigates the issue in **W+R+R-REV**, it does not restore correctness in general.

**Example 5** To see why, consider the program below where T<sub>2</sub> and T<sub>3</sub> share their code, along with one of its representative executions.

$$\begin{array}{l} T_1: a := y \\ T_2: r_2 := x \\ \quad x := 1 \\ \quad y := 1 \\ T_3: r_3 := x \\ \quad x := 1 \\ \quad y := 1 \end{array} \quad (R+RWW+RWW)$$


Assuming that we schedule all threads in a left-to-right manner, execution **42** cannot be generated by the procedure described so far. The first point where the algorithm has more than one choice to consider is the addition of R(x) of T<sub>3</sub>. The case where R(x) reads from W(x, 1) cannot lead to **42** because the restriction of the graph upon the revisit of R(y) will preserve the **rf**-edge of the R(x) read. Therefore, we are left with the case where R(x) reads from *init* (graph **K** below).



When the W(x, 1) of T<sub>3</sub> is added to **K**, there are three options:

- L**: W(x, 1) is added **co**-after T<sub>2</sub>'s W(x, 1). This execution is explored by DPOR, but cannot lead to the graph **42** because when W(y, 1) is added in T<sub>3</sub>, it will be unable to revisit R(y) because the W(x, 1) of T<sub>2</sub> is not maximally added w.r.t. T<sub>3</sub>'s W(y, 1): it is **co**-before T<sub>3</sub>'s W(x, 1), which is in T<sub>3</sub>'s **porf**-prefix.



- M**:  $W(x, 1)$  is **co**-before  $T_2$ 's  $W(x, 1)$ . This execution is dropped because **co** contradicts thread-order of symmetric events.
- N**:  $W(x, 1)$  revisits the  $R(x)$  of  $T_2$ . This execution is also dropped because it is not a representative one ( $T_2$  is reading a **co**-earlier value than  $T_3$ ).

As the **R+RWV+RWV** example above clearly demonstrates, fixing the scheduling policy is insufficient to guarantee completeness. Essentially, the issue described in §2.2.2 still persists: execution 42 could not be produced because a maximal extension was dropped (graph **M**) in favor of the representative one (graph **L**). In turn, in the representative execution **L**, a **co**-edge from a symmetric thread to the **porf**-prefix of the revisiting write precluded the revisit.

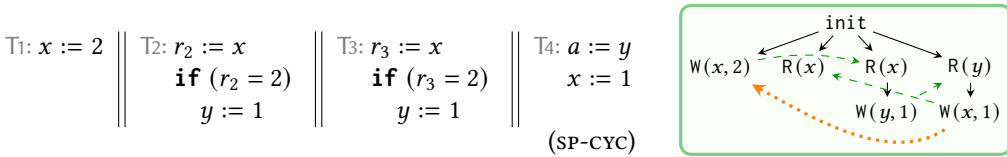
This last observation is key in marrying DPOR and SR: since a revisit fails due to an event of a symmetric thread being added non-maximally, SPORE's solution is to consider symmetric events part of the revisiting write's prefix. In the case of **R+RWV+RWV**, when SPORE considers the revisit between the  $W(y, 1)$  of  $T_3$  and the  $R(y)$  of  $T_1$ , the **prefix** of  $W(y, 1)$  will include not just the events **porf**-before it, but also the **porf**-prefix of symmetric events as well (namely, event  $W(x, 1)$  of  $T_2$ ). As such, graph 42 will be generated from **L** because all the affected events (namely,  $T_1$ 's  $R(y)$  and  $T_2$ 's  $W(x, 1)$ ) are added maximally w.r.t. the **new prefix** of  $W(y, 1)$ .

**2.2.4 Problem #3: Handling  $po \cup rf \cup co$  cycles.** Changing the notion of a prefix is instrumental in restoring completeness, but comes with a caveat. In DPOR, a write can never revisit events in its own prefix. So, by introducing a new notion of a prefix (henceforth **sprefix**) in SPORE, do we lose any executions? Is it possible that this novel notion of a prefix precludes some revisit that does not create a causal cycle, thereby rendering SPORE incomplete?

The answer depends on the underlying memory model. First, we can show that **sprefix** cycles boil down to  $po \cup rf \cup co$  cycles. (Our full argument is presented in §3.) Strong models, such as SC, TSO [SPARC International Inc. 1994], and SRA [Lahav et al. 2016], forbid  $(po \cup rf \cup co)^+$  cycles, and so it is never possible for a read to read from a write in its **sprefix**.

In weaker models, such as RC11 [Lahav et al. 2017], however, the answer is yes: it *can* be the case that an event is in its own **sprefix** but not in its own **porf**-prefix. Such a scenario is shown below.

**Example 6** Consider the **SP-CYC** program, where  $T_2$  and  $T_3$  share their code.



In the execution of Example 6,  $W(x, 1)$  is in its own **sprefix** ( $W(x, 1)$  is read from the  $R(x)$  of  $T_2$ , which is symmetric to the  $R(x)$  of  $T_3$ , which is in turn in the prefix of  $W(x, 1)$ ), but not in its own **porf**-prefix (there is no **porf** cycle).

To restore completeness, SPORE therefore checks that no consistent execution graph has a  $po \cup rf \cup co$  cycle. This condition typically holds: a  $po \cup rf \cup co$  cycle implies that there exist two writes that are not **porf**-ordered, and such unordered concurrent writes are rare in realistic implementations [Abdulla et al. 2019; Kokologianakis et al. 2019b]. As we show in §4, SPORE is directly applicable to realistic libraries of concurrent data structures.

```

enqueue( $v$ )  $\triangleq$ 
   $node := \text{malloc}(\dots)$ 
   $node.value := v$ 
   $node.next := \text{NULL}$ 
  do
     $t := \underline{tail}$ 
     $next := t.next$ 
    if ( $t \neq \underline{tail}$ ) continue
    if ( $next \neq \text{NULL}$ )
      CAS( $\underline{tail}, t, next$ )
    continue
  while ( $\neg \text{CAS}(t.next, next, node)$ )
  CAS( $\underline{tail}, t, node$ )

dequeue()  $\triangleq$ 
  do
     $h := \underline{head}$ 
     $n := h.next$ 
    if ( $h \neq \underline{head}$ ) continue
    if ( $n = \text{NULL}$ ) return None
  while ( $\neg \text{CAS}(\underline{head}, h, n)$ )
   $t := \underline{tail}$ 
  if ( $h = t$ )
    CAS( $\underline{tail}, t, n$ )
   $v := n.value$ 
  reclaim( $h$ )
  return  $v$ 

rdcss_read( $a_2$ )  $\triangleq$ 
   $r := a_2$ 
  while (is_desc( $r$ ))
    complete( $r$ )
   $r := a_2$ 
  return  $r$ 

complete( $d$ )  $\triangleq$ 
   $r := d.a_2$ 
   $n := (r = d.o_1) ?$ 
     $d.n_2 : d.o_2$ 
  CAS( $d.a_2, d, n$ )

rdcss( $d$ )  $\triangleq$ 
   $r := \text{CAS}(d.a_2, d.o_2, d)$ 
  while (is_desc( $r$ ))
    complete( $r$ )
   $r := \text{CAS}(d.a_2, d.o_2, d)$ 
  if ( $r = d.o_2$ ) complete( $d$ )
  return  $r$ 

```

Fig. 2. DGLM queue (left) and RDCSS (right). Global variables are underlined; function arguments are passed by reference; CAS returns whether it succeeded.

### 2.3 SPORE: Internal Symmetries

We now switch gears and present how SPORE exploits internal symmetries. We first present some examples of such symmetries (§2.3.1), and then discuss SPORE’s treatment (§2.3.2). We end this section by discussing how internal and thread-level symmetries interact (§2.3.3).

**2.3.1 Internal Symmetry Examples.** Fig. 2 shows two examples of internal symmetries: the Doherty-Groves-Luchangco-Moir (DGLM) queue [Doherty et al. 2004] and Restricted Double-Compare Single Swap (RDCSS) [Harris et al. 2002].

DGLM queue is a lock-free queue comprising two pointers *head* and *tail*. At the end of each enqueue operation, each enqueuer advances the *tail* pointer to point to the last element of the queue. If, however, a concurrent enqueuer or dequeuer detects that the *tail* pointer is lagging behind (i.e.,  $\underline{tail}.next \neq \text{NULL}$ ), it tries to advance *tail* on behalf of an incomplete enqueue.

RDCSS is a double CAS operation that takes as an argument a descriptor  $d$  containing two addresses  $a_1, a_2$  with their expected values  $o_1, o_2$  and a new value  $n_2$ . If both addresses contain their expected values, then the new value  $n_2$  is stored at the second address  $a_2$ . To perform the double comparison atomically, RDCSS first tries to place its descriptor in the  $a_2$  address, and then reads  $a_1$  to determine whether to replace it with the new value  $n_2$  or restore the old value  $o_2$ . In case another thread encounters the descriptor, it tries to complete the ongoing RDCSS call.

Both algorithms employ the textbook *helping pattern* [Herlihy 1991; Herlihy and Shavit 2008], where some operation A observes an ongoing, incomplete operation B and tries to complete B before performing its own. This helping pattern appears ins widely used concurrent libraries, including libcds [Khizhinsky n.d.], folly [Facebook n.d.] and ckit [Bahra n.d.], as well as in most algorithms described by Herlihy and Shavit [2008];

Observe that in both cases, the highlighted *main* and *helping* operations are *idempotent*: one of the CASes succeeds and all the others fail without changing the state. Moreover, their result is the same irrespective of which operation succeeds, and that the program cannot distinguish *which* operation succeeded. Indeed: (i) both operations execute exactly the same code, (ii) their returned value is not checked by the program, and (iii) swapping which of the operations succeeded preserves consistency and does not mask any error. As we will shortly see, these three conditions enable SPORE to exploit internal symmetries and drastically reduce the state space. (In contrast,

thread-level symmetries are inapplicable because the main and the helping operations have different execution prefixes.)

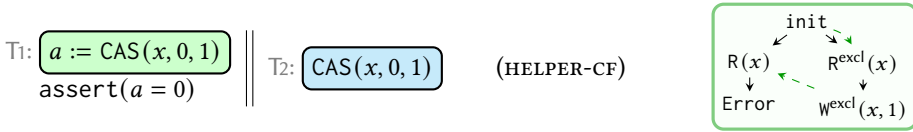
**2.3.2 Exploiting Idempotent Operations.** SPORE exploits idempotent operations by only exploring executions where the `main` operation succeeds. To this end, SPORE changes the underlying memory model and treats `helping` operations as no-ops, which have no incoming/outgoing `rf` or `co` edges. To do that, SPORE requires assistance from the user: the user annotates helping operations in the program (as in Fig. 2), and then SPORE automatically treats them as no-ops and reduces the state space to be searched.

Annotations bring us to a major challenge that needs to be resolved: ensuring annotation correctness. If users incorrectly annotate a function as helping, it might mask an existing error in the user program. As such, SPORE uses a *dummy event* in the place of the function to check whether certain (sufficient) conditions hold. If they do not, SPORE reports an annotation error to the user.

Some minimal preconditions that need to hold for a function  $f_h$  to be considered as helping w.r.t. a function  $f_m$  have already been stated in §2.3.1: (i)  $f_h$  and  $f_m$  execute the same code, (ii) the returned value of  $f_h$  and  $f_m$  is not checked by the program, and (iii) replacing an execution where  $f_m$  fails and  $f_h$  succeeds with one where  $f_m$  succeeds and  $f_h$  is treated as no-op preserves consistency and the presence of an error.

Let us now go over these conditions in more detail. The first two conditions lie at the heart of idempotency, and are what allow SPORE to treat  $f_h$  as a no-op: no code uses the result of  $f_h$  and is thus safe to disregard it. Had  $f_h$  and  $f_m$  been different (or had their results been used), then annotating one of them as helping would mask errors in programs, like in the example below.

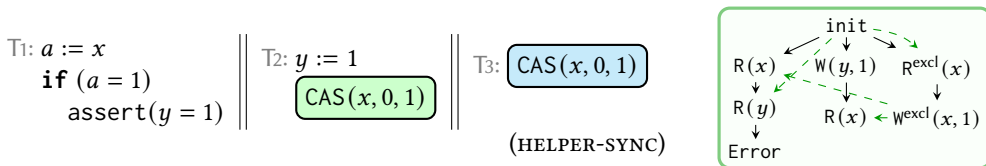
**Example 7** Consider the `HELPER-CF` program, along with one of its execution graphs.



$f_m$  and  $f_h$  are functions comprising a single CAS operation, but the result of  $f_m$  is used (i.e.,  $f_h$  is incorrectly annotated as helping). If we treat  $f_h$  as a dummy event, the execution above (where the failed CAS generates a single read event and the successful one two events annotated with an `excl` flag) will not be explored and the error will be missed.

Condition (iii) is a bit more intricate. To ensure it, we need to guarantee that in any execution where  $f_h$  succeeds,  $f_m$  has already observed (in a synchronizing manner) the operations of  $f_h$ . If reading from writes in  $f_m$  can imply less synchronization with the rest of the program, then it is possible that reading from  $f_h$  results in an error, but reading from  $f_m$  does not (and thus, treating  $f_h$  as dummy can mask errors). We demonstrate this point with the following example.

**Example 8** Consider the `HELPER-SYNC` program under SC.



If the CAS in  $T_2$  succeeds and  $T_1$ 's read of  $x$  reads from it, then  $T_1$  will necessarily read  $y = 1$ . If, however, the CAS in  $T_3$  succeeds and  $T_1$  reads from it (as shown in the graph above),  $T_1$  can subsequently read  $y = 0$  and violate its assertion (as shown in the graph above).

To fix this last issue, SPORE imposes four more conditions on the user annotations:

- (1)  $f_m$  and  $f_h$  have no other writes apart from a final CAS
- (2)  $f_m$  has a preceding *source event* whose value it uses as the compare operand
- (3)  $f_m$  is immediately preceded by a write, which is observed in a synchronizing manner before  $f_h$
- (4) all writes to the location of  $f_m$ 's CAS are part of *read-modify-write* (RMW) operations

These conditions are formalized in §3. As we prove in §3, these conditions are sufficient to detect erroneously annotated helping patterns.

**2.3.3 The Interaction Between Internal and Thread-Level Symmetries.** Before moving on to our formal discussion of SPORE, it is worth noting that idempotent operations *facilitate* SR. Consider an example with two symmetric threads performing a helping CAS. Assuming that the threads are symmetric up until the CASes, treating the CASes as an RMW operations breaks the symmetry, while treating them as dummy events preserves the symmetry.

### 3 SPORE: Formal Description

In this section, we describe the theoretical basis of SPORE. In particular, we explain: (§3.1) the representation of executions as execution graphs; (§3.2) how SPORE can be represented as a memory model; (§3.3) SPORE's exploration algorithm; (§3.4) why SPORE is correct, i.e., why it explores exactly one graph per the combined equivalence classes of DPOR and SR, and does not mask any errors.

#### 3.1 Execution Graphs

An execution graph comprises a set of events (nodes), and a few relations on these events (edges).

*Definition 3.1.* An event,  $e \in \text{Event}$ , is either the initialization event `init`, or a thread event  $\langle t, i, l \rangle$  where  $t \in \text{Tid}$  is a thread identifier,  $i \in \text{Idx}$  is a serial number (denoting the index of an event within a thread), and  $l \in \text{Lab}$  is a label that takes (at least) one of the following forms:

- Write label:  $W^k(l, v) \in \mathbb{W}$ , where  $k$  records the write attributes,  $l \in \text{Loc}$  the location accessed, and  $v \in \text{Val}$  the value written.
- Read label:  $R^k(l, v) \in \mathbb{R}$ , where  $k$  records the read attributes,  $l \in \text{Loc}$  the location accessed, and  $v \in \text{Val}$  the value read.
- Annotated function label:  $M^m(f, as) \in \mathbb{M}$ , where  $m \in \{\text{main, help}\}$  is the function attribute,  $f \in \text{Fname}$  is the name of the function been called, and  $as \in \text{Val}^*$  is a sequence representing the function arguments.

Read and write attributes include the exclusivity flag `excl` for RMWs, and the access mode for RC11-style models. (Additional kinds of events exist for memory allocations, deallocations, assertion violations, *etc.*, but these do not affect the model checking algorithm in any meaningful way.)

Having defined events, we define execution graphs as follows.

*Definition 3.2.* An execution graph  $G \in \text{Exec}$  comprises the following components:

- (1) a set of events  $E$  that includes `init` and does not contain multiple events with the same thread identifier and serial number;
- (2)  $\text{rf} : E \cap \mathbb{R} \rightarrow E \cap \mathbb{W}$ , called the *reads-from* function, mapping each read event to a same-location write from where it gets its value;

- (3)  $\text{co} \subseteq \bigcup_{l \in \text{Loc}} W_l \times W_l$  (where  $W_l \triangleq \{\text{init}\} \cup \{\langle t, i, l \rangle \in E \mid l = W-(l, \_)\}$ ) called the *coherence order*, a strict partial order that is total on  $W_l$  for every location  $l \in \text{Loc}$ ; and
- (4)  $\leq$ , a total order on  $E$  that represents the order in which events were incrementally added to the graph.

### Conventions

We write  $G.E$ ,  $G.\text{rf}$ ,  $G.\text{co}$  and  $\leq_G$  to project the various components of an execution graph. Given two events  $e_1, e_2 \in G.E$ , we write  $e_1 <_G e_2$  if  $e_1 \leq_G e_2$  and  $e_1 \neq e_2$ . In relational algebra expressions, we abuse notation and write  $G.\text{rf}$  for the relation  $\{\langle G.\text{rf}(r), r \rangle \mid r \in G.R\}$ .

We assume that  $\text{init} \in W$ , and omit the  $\emptyset$  for read/write labels with no attributes.

The functions  $\text{tid}$ ,  $\text{idx}$ ,  $\text{loc}$ ,  $\text{mod}$  and  $\text{arg}$  respectively return the thread identifier, serial number, location, access mode and function arguments of an event, when applicable.

We write  $G.W$  for  $G.E \cap W$  (and similarly for other sets), and use superscript and subscripts to restrict label sets (e.g.,  $W_l \triangleq \{\text{init}\} \cup \{w \in W \mid \text{loc}(w) = l\}$ ).

Observe that  $G$  does not have an explicit *program order* ( $\text{po}$ ) component. We induce  $\text{po}$  based on our representation of events as follows:

$$\text{po} \triangleq \{\langle \text{init}, e \rangle \mid e \in \text{Event} \setminus \{\text{init}\}\} \cup \{\langle \langle t_1, i_1, l_1 \rangle, \langle t_2, i_2, l_2 \rangle \rangle \mid t_1 = t_2 \wedge i_1 < i_2\}$$

In our technical appendix [Kokologiannakis et al. 2024b], we define two mappings from programs to sets of execution graphs: (1)  $\llbracket \cdot \rrbracket$ , which ignores function annotation labels, and simply generates an event with a  $M^m$  label before the events corresponding to the function body; and (2)  $\llbracket \cdot \rrbracket^{\text{Annot}}$ , which in the case of functions annotated with *help*, generates only the  $M^{\text{help}}$  event and does not generate any events for the body of the function call. Both mappings keep the  $\text{rf}$  and  $\text{co}$  components of graphs completely unconstrained. These components will be constrained by the memory model.

### 3.2 Consistency and Error Detection

A memory model,  $M$ , comprises three components: (a) a *causal prefix* relation,  $\text{cb}_M$ , (b) a *consistency predicate*  $\text{consistent}_M(G)$  that determines whether an execution graph  $G$  is consistent, and (c) an  $\text{ISERRONEOUS}_M(G)$  predicate, prescribing whether  $G$  contains an error (e.g., an invalid memory access) according to  $M$ .

The consistency predicate is used to constrain the semantics of a program. The annotation-ignoring (resp. annotation-aware) semantics of a program  $P$  under a memory model  $M$ , denoted  $\llbracket P \rrbracket_M$  (resp.  $\llbracket P \rrbracket_M^{\text{Annot}}$ ), is given by the set of execution graphs in  $\llbracket P \rrbracket$  (resp.  $\llbracket P \rrbracket^{\text{Annot}}$ ) that are  $M$ -consistent.

In SPORE, we assume an underlying memory model  $M$  with  $\text{cb}_M = (\text{po} \cup \text{rf})^+$ ,  $\text{consistent}_M(\cdot)$  being *extensible*, *prefix-closed*, and implying RMW atomicity and  $\text{cb}_M$ -acyclicity [Kokologiannakis et al. 2022], and  $\text{ISERRONEOUS}_M(\cdot)$  being *prefix-monotone*. Models satisfying these requirements include SC [Lamport 1979], TSO [SPARC International Inc. 1994], Release-Acquire (RA) [Lahav et al. 2016], and RC11 [Lahav et al. 2017]. We then define a new memory model, SYM, with

$$\begin{aligned} \text{cb}_{\text{SYM}} &\triangleq (\text{po} \cup \text{rf} \cup \text{symb})^+ \\ \text{consistent}_{\text{SYM}}(G) &\triangleq \text{consistent}_M(G) \wedge \text{IRREFLEXIVE}(\text{symb}; \text{eco}) \\ \text{ISERRONEOUS}_{\text{SYM}}(G) &\triangleq \text{ISERRONEOUS}_M(G) \vee \neg \text{IRREFLEXIVE}((\text{po} \cup \text{rf} \cup \text{co})^+) \\ &\vee G \text{ is incorrectly annotated (see Def. 3.3 below)} \end{aligned}$$

where  $G.\text{symb}$  is the *symmetry-before* order that orders prefix-matching events according to their thread order. Concretely,  $\langle e_1, e_2 \rangle \in G.\text{symb}$  if the following hold:

- (i)  $\text{idx}(e_1) = \text{idx}(e_2)$  and  $\text{tid}(e_1) < \text{tid}(e_2)$
- (ii)  $e_1$  and  $e_2$  originate from threads running the same code (and spawned consecutively),
- (iii) have no preceding same-thread writes, and
- (iv) for every preceding same-thread read  $r_1$  of  $e_1$ , the corresponding (i.e., having the same index) read  $r_2$  in  $\text{tid}(e_2)$  has the same  $\text{rf}$  (i.e.,  $G.\text{rf}(r_1) = G.\text{rf}(r_2)$ ).

*Annotation Correctness.* To ensure annotation correctness, SPORE first checks that for each  $f_h \in G.M^{\text{HELP}}$ , there exists a (unique)  $f_m \in G.M^{\text{main}}$  with the same arguments, and that these functions do not return any results (cf. conditions (i) and (ii) of §2.3.2), and are well-formed: they comprise a (possibly empty) sequence of reads followed by a CAS operation, with a possible data dependency from the reads to the CAS (no other dependencies are allowed so that the locations accessed can be deduced by the arguments of  $f_m/f_h$ ).

Assuming both functions has the proper form, SPORE has to now ensure that (iii) holds, i.e., that their synchronization is the same. Since the definition of synchronization differs among memory models, for simplicity, we here provide a definition that works for SC and RA<sup>4</sup>. In what follows, we lift  $\text{loc}/\text{exp}$  to return the location/expected-value of the CAS read following an  $f_m \in G.M^{\text{main}}$ .

Our definition uses the notion of a *source write*  $s$  at location  $\text{loc}(f_m)$ , which is observed before  $f_m$  (i.e., either it is po-before  $f_m$  or it is read po-before  $f_m$ ), and writes the value  $\text{exp}(f_m)$ . We also require that the immediate po-predecessor of  $f_m$  is observed before  $f_h$ , which ensures that the  $f_h$  has synchronized with everything in  $f_m$ 's prefix, and that all writes to  $\text{loc}(f_m)$  after  $s$  are RMWs and do not write the same value as  $s$ . The latter condition ensures that  $f_m$  and  $f_h$  cannot both succeed, and that if  $f_h$  succeeds, then  $f_m$  observes its update.

*Definition 3.3 (Annotation correctness).* An execution  $G$  is *correctly annotated* if for all  $f_h \in G.M^{\text{help}}$ , there exist (a) a corresponding  $f_m \in G.M^{\text{main}}$  with  $\text{arg}(f_m) = \text{arg}(f_h)$  and (b) a source write  $s \in G.W$  with  $\text{loc}(s) = \text{loc}(f_m)$  and  $\text{val}(s) = \text{exp}(f_m)$  such that:

- $\langle s, f_m \rangle \in G.\text{rf}^?$ ; po ( $s$  is observed before  $f_m$ ),
- $\langle f_m, f_h \rangle \in \text{po}^{-1}|_{\text{imm}}; G.\text{rf}$ ; po (the immediate predecessor of  $f_m$  is observed before  $f_h$ ),
- for all  $w \in \text{rng}([s]; \text{co})$ ,  $w \in W^{\text{excl}}$  and  $\text{val}(w) \neq \text{val}(s)$  (all subsequent writes to  $\text{loc}(f_m)$  are RMWs and write different values).

### 3.3 Exploration Algorithm

Let us now proceed by showing how SPORE enumerates all SYM-consistent execution graphs of a program  $P$ . The algorithm is shown in Algorithm 1, which constructs the consistent graphs incrementally by recording the event addition order in the graphs'  $\leq_G$  component. SPORE is optimal in the sense that it only explores consistent execution graphs and it never explores two execution graphs that differ only in their  $\leq_G$  components.

SPORE verifies the input program  $P$  under a memory model  $M$  by calling EXPLORE with the initial graph  $G_0$  containing only the initialization event `init`.

First, EXPLORE( $P, G$ ) checks whether the current graph contains an error (Line 2). Note that errors are checked against SPORE's memory model: they include not only errors under the underlying memory model  $M$ , but also *user annotation errors*.

In addition, recall that SPORE's errors include the existence of  $\text{po} \cup \text{rf} \cup \text{co}$  cycles. Such a check is necessary to justify why exploring  $\text{cb}_{\text{SYM}}$ -acyclic execution graphs suffices: any  $(\text{po} \cup \text{rf} \cup \text{co})$ -acyclic graph where the symmetry-before order does not contradict the  $\text{eco}$  order is also  $\text{cb}_{\text{SYM}}$ -acyclic.

<sup>4</sup>In our technical appendix [Kokologiannakis et al. 2024b], we provide the definition for the RC11 memory model. The definition for SC/RA is a special case of the RC11 definition.

**Algorithm 1** SPORE: An optimal combination of DPOR and SR

---

```

1: procedure EXPLOREP( $G$ )
2:   if ISERRONEOUSSYM( $G$ ) then exit("Error")
3:    $a \leftarrow$  ADDNEXTEVENTP( $G$ )
4:   if  $a \in R$  then
5:     for  $w \in G.W_{loc(a)}$  do EXPLOREIFCONSISTENTP(SetRF( $G, a, w$ ))
6:   else if  $a \in W$  then
7:     EXPLORECOSP( $G, a$ )
8:     for  $r \in G.R_{loc(a)}$  such that  $\langle r, a \rangle \notin G.cb_{SYM}$  do
9:       Deleted  $\leftarrow$   $\{e \in G.E \mid r <_G e <_G a \wedge \langle e, a \rangle \notin G.cb_{SYM}\}$ 
10:      if SHOULDREVISIT( $G, \langle r, a, Deleted \rangle$ ) then
11:        EXPLORECOSP(SetRF( $G \setminus Deleted, r, a$ ),  $a$ )
12:   else if  $a \neq \perp$  then
13:     EXPLOREP( $G$ )

14: procedure EXPLOREIFCONSISTENTP( $G$ )
15:   if consistentSYM( $G$ ) then EXPLOREP( $G$ )

16: procedure EXPLORECOSP( $G, a$ )
17:   for  $w_p \in G.W_{loc(a)}$  do EXPLOREIFCONSISTENTP(SetCO( $G, w_p, a$ ))

```

---

If the graph is error-free, EXPLORE extends it by one event  $a$  from the program by calling ADDNEXTEVENT (Line 3). If there are no events to add, then a full execution of  $P$  has been explored, and EXPLORE returns.

If  $a$  is a read, then EXPLORE recursively explores all consistent rf options for that read. As such, for each same-location write  $w$ , EXPLORE recursively calls itself (via the helper function EXPLOREIFCONSISTENT) on the graph that results if  $a$  reads from  $w$  (Line 5). EXPLOREIFCONSISTENT checks whether  $G$  is consistent (Line 15), and if so calls EXPLORE recursively. (Recall that consistency also requires that the graph does not violate our SR principle.)

If  $a$  is a write, SPORE proceeds with the non-revisit case and the revisit case, respectively. For the non-revisit case, EXPLORE checks for all possible placements of the newly added write in co by means of EXPLORECOs (Line 7).

For the revisit case, SPORE also checks whether any of the existing reads of  $G$  can be *revisited* to read from  $a$ : since  $a$  was not present when their possible reads-from options were examined, EXPLORE explores these additional rf options now. Thus, for each same-location read  $r$  that does not precede  $a$ , if revisiting  $r$  will not lead to a duplicate exploration (checked by SHOULDREVISIT<sup>5</sup>), EXPLORE calls EXPLORECOs on the graph that occurs if all the events that were added after  $r$  are deleted, excluding  $a$  and its predecessors (Line 11).

Observe, however, that as we motivated earlier in §2.2.4, SPORE only explores cb<sub>SYM</sub>-acyclic execution graphs. As such, SPORE never revisits reads that are in cb<sub>SYM</sub>-before  $a$  (as opposed to cb<sub>M</sub>-before  $a$ ), as revisiting such reads would create cb<sub>SYM</sub> cycles (the cb<sub>SYM</sub>-prefix of a revisiting write is always preserved).

If  $a$  has any other type (Line 13), EXPLORE recursively calls itself.

<sup>5</sup>As the definition of SHOULDREVISIT is unnecessary for this discussion, we omit it; we refer interested readers to our technical appendix [Kokologiannakis et al. 2024b].

*Remark 1.* Observe that, with the exception of annotation errors, *SPORE* does not take any special care for method annotation labels  $M$ . Indeed, this is because these are handled implicitly by the interpreter: Line 3 adds events according to our annotated semantics  $\llbracket P \rrbracket^{\text{Annot}}$ . When the interpreter encounters a function annotated with *main*, it will yield an  $M^{\text{main}}(as)$  (which is not treated specially) as well as the events of the function, while for a function annotated with *help* it will only yield an  $M^{\text{help}}(as)$  event.

*Remark 2.* We assume that the `ADDNEXTEVENT` procedure (Line 3), always picks the leftmost thread among the ones that are symmetric, i.e., their next events are prefix-matching. This is necessary for the algorithm's correctness, which demands that when an event  $e$  is added, its `cbSYM`-prefix already be present in the graph.

### 3.4 Soundness, Completeness and Optimality

*3.4.1 Soundness of Internal Symmetries.* We show that if a program  $P$  is erroneous under its standard interpretation  $\llbracket P \rrbracket$  (which ignores annotations), then it is also erroneous under the annotated interpretation  $\llbracket P \rrbracket^{\text{Annot}}$  (which encodes annotated functions with dummy events). See [Kokologiannakis et al. 2024b] for how programs are mapped to execution graph sets.

**THEOREM 3.4.** *Let  $P$  be an annotated program and  $G \in \llbracket P \rrbracket_M$  such that  $\text{ISERRONEOUS}_M(G)$ . Then, there exists  $G' \in \llbracket P \rrbracket_M^{\text{Annot}}$  such that  $\text{ISERRONEOUS}_{\text{SYM}}(G)$ .*

**PROOF SKETCH.** It suffices to show that there exists a corresponding execution  $G'$  (where every  $f_h$  being treated as a (single) dummy event  $M^{\text{help}}(\dots)$ ) such that (1)  $\text{ISERRONEOUS}_M(G')$  holds, or (2)  $G'$  is incorrectly annotated (see Def. 3.3). The lack of an annotation error is essential in showing that changing  $G'$  so that  $f_m$  succeeds instead of  $f_h$  does not affect  $G'$ 's consistency.

The conditions of Def. 3.3 essentially enforce that in any execution where  $f_h$  would succeed, (a) there is an  $f_m$ , running the same code, (b)  $f_m$  fails (there can only be one write that writes the expected value), (c)  $f_m$  reads from the CAS of  $f_h$ , or from a `co`-later (due to coherence and the presence of the source event), and therefore there is a `porf`-path from the CAS of  $f_h$  to the CAS of  $f_m$  (all writes to the CAS location are part of an RMW, and thus such a `co` path is also a `porf` path), (d)  $f_m$  is preceded by a write that was observed by the thread of  $f_h$ . This guarantees that swapping the events of  $f_m$  with those of  $f_h$ , and replacing the events of  $f_h$  with a no-op, adds no synchronization in the execution, and therefore preserves both consistency and the presence of an error.

If any of the previous conditions fails, we show that there exists an execution with  $f_h$  being treated as a no-op that is not correctly annotated.  $\square$

*3.4.2 Correctness of SPORE.* To state our desired result, we first need to formally define which are the execution graphs that are considered equivalent up to symmetry. Given a program  $P$  with  $N$  threads, a *valid thread permutation*  $\pi$  is a bijection  $\{1, \dots, N\} \mapsto \{1, \dots, N\}$  such that threads  $\pi(i)$  and  $i$  share the same code for all  $1 \leq i \leq N$ . We say that two executions  $G_1$  and  $G_2$  are *symmetric*, denoted  $G_1 \approx G_2$ , if there exists a valid thread permutation  $\pi$  such that  $\pi(G_1) = G_2$ , where  $\pi(G_1)$  applies the permutation to all the thread IDs in the events of  $G_1$ .

The following proposition demonstrates that the class of  $M$ -consistent execution graphs up to symmetry corresponds (one-to-one) to the class of  $\text{SYM}$ -consistent execution graphs.

**PROPOSITION 3.5.** *Given a program  $P$  and an execution graph  $G \in \llbracket P \rrbracket_M^{\text{Annot}}$ , there is a unique execution graph  $G' \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  such that  $G \approx G'$ .*

**PROOF.** To obtain  $G'$  from  $G$ , sort the threads running the same function by the `eco` of the respective events (lexicographically, in po order). It is easy to see that this ordering is well-defined



(there are no cycles), and unique: any possibly **eco**-unordered threads are in fact equal, and that the constructed graph  $G'$  satisfies  $\text{IRREFLEXIVE}(\text{ symb; eco})$ .  $\square$

Correctness of the exploration algorithm follows by adapting the proof of AWAMOCHÉ [Kokologianakis et al. 2023] and is captured by the following proposition.

**PROPOSITION 3.6 (ALGORITHMIC CORRECTNESS AND OPTIMALITY).**

- (1)  $\text{EXPLORE}_P(G_0)$  terminates.
- (2)  $\text{EXPLORE}_P(G_0)$  only explores  $\text{cb}_{\text{SYM}}$ -prefixes of executions in  $\llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$ .
- (3)  $\text{EXPLORE}_P(G_0)$  explores every execution  $G \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  such that  $\text{IRREFLEXIVE}(G.\text{cb}_{\text{SYM}})$ .
- (4)  $\text{EXPLORE}_P(G_0)$  never explores the same  $G$  twice.

Termination holds because either a revisit step is performed and the part of the graph that cannot be changed grows or a non-revisit step is performed and the execution graph grows. Soundness holds by construction because consistency is checked before every recursive call. Completeness is more elaborate: it holds because all possible **rf/co** options are considered for each newly added event, and moreover previous reads can be revisited in their maximal extension (which always exists and is consistent). Optimality holds because there cannot be two steps leading to the same graph; in case of revisits, that is precluded by the uniqueness of maximal extensions.

We next show that if  $\llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  includes a  $\text{cb}_{\text{SYM}}$ -cyclic execution, which the algorithm would not explore, then it also includes a  $\text{cb}_{\text{SYM}}$ -acyclic execution with a  $\text{po} \cup \text{rf} \cup \text{co}$  cycle, which the algorithm would explore and report.

**PROPOSITION 3.7 ( $\text{cb}_{\text{SYM}}$  CYCLE).** *If there is an execution  $G \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  with a  $G.\text{cb}_{\text{SYM}}$  cycle, then there is an execution  $G' \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  such that  $\text{IRREFLEXIVE}(G'.\text{cb}_{\text{SYM}})$  and  $G'$  has a  $\text{po} \cup \text{rf} \cup \text{co}$  cycle.*

Combining Prop. 3.5, Prop. 3.6(3), and Prop. 3.7, we obtain our completeness result.

**THEOREM 3.8 (COMPLETENESS).** *If there exists  $G \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  such that  $\text{ISERRONEOUS}_{\text{SYM}}(G)$ , then  $\text{EXPLORE}_P(G_0)$  will report an error. Otherwise, for each  $G \in \llbracket P \rrbracket_M^{\text{Annot}}$ ,  $\text{EXPLORE}_P(G_0)$  will explore an execution  $G' \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  such that  $G \approx G'$ .*

Combining Prop. 3.5 and Prop. 3.6(4), we obtain our optimality result.

**THEOREM 3.9 (OPTIMALITY).** *For any two executions  $G$  and  $G'$  explored by  $\text{EXPLORE}_P(G_0)$ ,  $G \neq G'$ .*

## 4 Evaluation

We implemented SPORE as a tool for C/C++ programs on top of the open-source GENMC stateless model checker, which implements the TRUST algorithm for DPOR. We reused GENMC's infrastructure for interpreting programs and constructing and maintaining execution graphs, but replaced GENMC's consistency checking and error detection mechanism with the ones described in §3.1. We also modified the notion of a prefix used in graph construction to use  $\text{cb}_{\text{SYM}}$ , and made GENMC's scheduler respect  $\text{cb}_{\text{SYM}}$  when encountering symmetric threads.

### 4.1 Goals

We evaluate SPORE on a set of real-world implementations with two goals: (1) show that SPORE scales well enough to verify useful implementations (and determine its scalability limit), and (2) determine to what extent its scalability should be attributed to internal vs thread-level symmetries.

To attain these goals, we run SPORE on a set of representative real-world clients and benchmarks. The clients evaluate the effectiveness of the SR algorithm, while the benchmarks evaluate the effectiveness of SPORE's modeling of internal symmetries. To further study how internal and

thread-level symmetries contribute to SPORE’s performance, we compare SPORE against (a) plain SMC enhanced with SR (SR), (b) a baseline TRUST implementation (TRUST), (c) SPORE without thread-level symmetries (DPOR+IS), and (d) SPORE without internal symmetries (DPOR+SR). Our evaluation is performed under RC11.

As we show, SPORE yields a huge improvement over the state-of-the-art as it can gracefully scale to up to 6 threads (often to many more), and both internal and thread-level symmetries are crucial for its scalability to more threads.

*Experimental Setup.* We conducted all experiments on a Dell PowerEdge R6525 system running a custom Debian-based distribution with 2 AMD EPYC 7702 CPUs (256 cores @ 2.80 GHz) and 2TB of RAM. We set the timeout limit to 30 minutes (denoted by ☹). All times are in seconds.

We also ran some of our benchmarks against the DPOR implementation of NIDHUGG [Abdulla et al. 2014], which obtained similar and/or worse results than TRUST (see [Kokologiannakis et al. 2024b]).

## 4.2 Benchmarks

To evaluate the effectiveness of thread-level symmetries, we used three different clients:

- $\text{Multiset}(N)$ :  $\lceil \frac{N}{2} \rceil$  (resp.  $\lfloor \frac{N}{2} \rfloor$ ) threads insert (resp. remove) elements at a data structure; the client checks whether each removed element was previously inserted.
- $\text{LIFO/FIFO}(N)$ : two threads check for the LIFO/FIFO property, while  $\lceil \frac{N}{2} \rceil$  (resp.  $\lfloor \frac{N}{2} \rfloor$ ) threads create “noise” in the queue to increase traffic, by inserting (resp. removing) elements.
- $\text{Empty}(N)$ :  $N$  threads insert an element and subsequently remove an element; the client ensures each removal succeeds.

As it can be seen, the clients become progressively more challenging in the sense that the number of multiple operations per thread increases, which hinders symmetry reduction.

To demonstrate that SPORE is applicable to non-data-structure benchmarks as well, we used two other clients (Fig. 4):

- $\text{Mutex}(N)$ :  $N$  threads perform a lock followed by an unlock operation.
- $\text{RDCSS}(N)$ :  $N$  threads perform an RDCSS call followed by an RDCS/read call, and 2 threads perform a single RDCSS call.

To evaluate the effectiveness of internal symmetries, we used some representative benchmarks both with and without idempotent operations:

- $\text{msqueue}$  [Michael and Scott 1998],  $\text{dglmqueue}$  [Doherty et al. 2004],  $\text{folqueue}$  [Fober et al. 2001] and  $\text{rdcss}$  [Harris et al. 2002] all employ idempotent operations.
- $\text{treiber}$  [Treiber 1986],  $\text{ttaslock}$  [Herlihy and Shavit 2008, §7.2] and  $\text{twalock}$  [Dice and Kogan 2019] do not employ idempotent operations.

These benchmarks exercise different aspects of internal symmetries so that the individual effects of each symmetry type are more visible.

We also note that we have identified idempotent operations in various widely used concurrency libraries (e.g.,  $\text{libcdfs}$  [Khizhinsky n.d.],  $\text{folly}$  [Facebook n.d.],  $\text{ckit}$  [Bhra n.d.]). Even though SPORE’s support for C++ precluded us from using  $\text{libcdfs}$  and  $\text{folly}$  as benchmarks, we did manage to run certain benchmarks from  $\text{ckit}$ , with similar performance gains.

## 4.3 Results

Our results are summarized in Fig. 3<sup>6</sup>. First, as explained in §1, SR alone is inadequate for scalability, and using a combination of DPOR and SR is crucial: with the exception of a few benchmarks, SR

<sup>6</sup>Detailed tables can be found in [Kokologiannakis et al. 2024b].

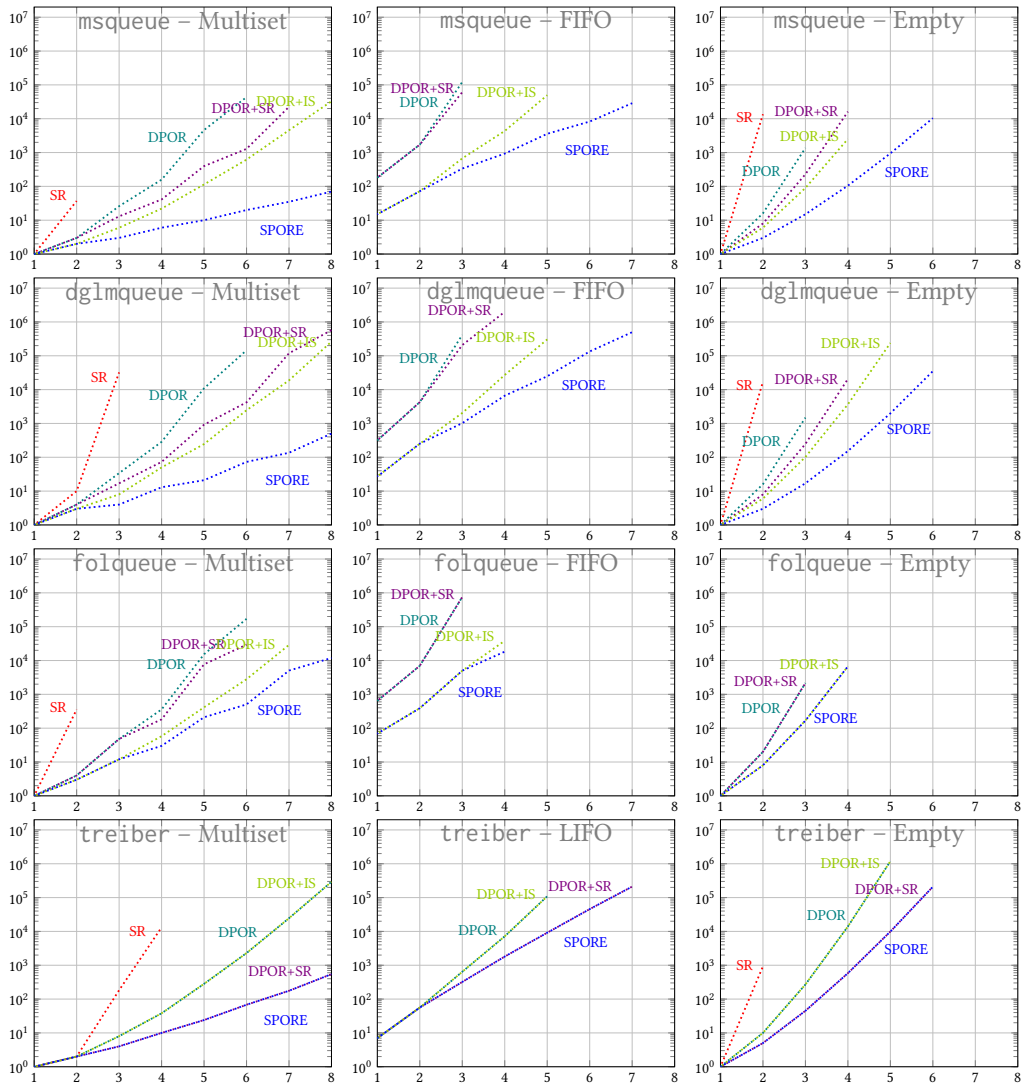


Fig. 3. Data structure benchmarks: Number of executions expored (Y-axis) per input parameter (X-axis)

consistently times out (and we therefore dismiss it for the rest of this discussion). Second, both thread-level and internal symmetries are crucial for scaling to more threads: exclusively either kind of symmetry typically leads to timeouts for some number of threads.

Let us now examine the benchmarks in more detail, starting with the multiset client (left column). The main takeaway from this client is immediately evident: while TRuSt typically scales up to 6 threads before timing out, SPORE scales gracefully to 8 threads (and more). Looking more closely, however, there are a few other interesting aspects as well.

Starting with *msqueue* and *dglmqueue*<sup>7</sup>, TRuSt times out for 6 threads and above, while SPORE can scale up to many more. The reason for that is simple: the CAS instruction present in the queue’s

<sup>7</sup>These benchmarks only differ in their dequeue method, which is why the results are very similar.

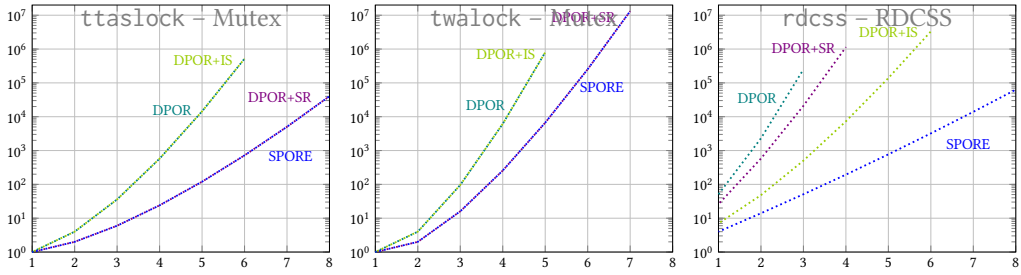


Fig. 4. Non-data-structure benchmarks: Number of executions explored (Y-axis) per input parameter (X-axis)

idempotent operation breaks symmetry, thereby leading to state-space explosion. SPORE, on the other hand, runs lickety-split: it explores a single execution when the client is fully symmetric (up to 4 threads), and a small number of executions otherwise (modeling the different ways insertions interfere with deletions). As the number of dequeuers increases, SPORE explores more executions, as there are more ways for deletions to interfere with insertions.

Moving on to *folqueue* and *treiber*, we can make observations similar to the ones for the previous benchmarks, albeit a bit toned down. In the case of *folqueue*, thread-level symmetries have a limited effect, as each thread uses a distinct (global) location to dispose pointers, which breaks symmetry among threads early: SPORE performs similarly to DPOR+IS, while TRUST performs similarly to DPOR+SR. Analogously, in *treiber*, internal symmetries have no effect, as the code has no idempotent operations: SPORE performs just as well as DPOR+SR, while DPOR+IS performs just as well as TRUST.

Generally, we observe that DPOR+IS performs better than DPOR+SR in the multiset client when both thread-level and internal symmetries are present, implying that internal symmetries carry more weight when it comes to scaling to more threads. This should not come as a surprise. Idempotent operations might be performed more than once per thread, while thread-level symmetry will break after the first non-symmetric operation. As such, since the number of idempotent operations is greater than the number of threads, internal symmetries offer a greater reduction.

Next, we move on to the other two clients. In a similar fashion, SPORE scales much better than TRUST (which only manages to terminate within the time limit for two or three configurations), although it does not manage to finish within the time limit for all configurations, since these clients are not completely symmetric (like the multiset one). As expected, SPORE performs better in the LIFO/FIFO (where it can better leverage the symmetry in the client), and DPOR+IS performs better than DPOR+SR whenever there are internal symmetries, for the same reasons as in the multiset client. (Note that SPORE performs similarly to DPOR+IS for the first configuration of each benchmark in the LIFO/FIFO client, as SR requires at least two symmetric threads to have any effect.)

Finally, in Fig. 4 we compare all tools on some non-data-structure benchmarks. The two locking benchmarks do not employ idempotent operations, and thus SPORE coincides with DPOR+SR, which has an exponentially smaller state-space than plain DPOR. In contrast, *rdcss* makes heavy use of idempotent operations, and so SPORE manages to scale way better than plain DPOR.

## 5 Related Work

As far as symmetry reduction is concerned, it has mostly been explored in the context of stateful model checking [Clarke et al. 1996; Emerson and Wahl 2005; Wahl and Donaldson 2010]. In that setting, the main challenge is to identify when two threads are symmetric, that is computationally

as hard as the graph isomorphism problem. By contrast, SPORE is able to detect when two threads are symmetric on-the-fly, though in principle the reductions it achieves are not as good as the ones in stateful model checking.

As far as internal symmetries are concerned, even though a lot of effort has been devoted into making DPOR algorithms more efficient and scalable during the past few years (e.g., [Abdulla et al. 2015, 2017, 2018; Aronis et al. 2018; Chalupa et al. 2017; Chatterjee et al. 2019; Kokologiannakis et al. 2017, 2022, 2019b; Nguyen et al. 2018; Norris and Demsky 2013; Rodríguez et al. 2015]), most works focus on improving the core of DPOR and do not take into consideration the programs under test. SAVER [Kokologiannakis et al. 2021] and LAPOR [Kokologiannakis et al. 2019a] extend DPOR for programs that have spinloops and locks, respectively, while constrained-DPOR [Albert et al. 2018] takes programmer annotations into account in order to consider certain atomic operations non-conflicting.

In a different context, there has been a large body of work on static verification of concurrent programs, with techniques such as bounded model checking (BMC) or abstraction-based techniques (e.g., [Clarke et al. 2004; Elmas et al. 2009; Flanagan et al. 2005; Gavrilenko et al. 2019]). We expect that—at least for SAT/SMT-based techniques—both thread-level and internal symmetries could be exploited in a similar fashion to reduce the size of the resulting SAT formula and speed up the verification.

## 6 Conclusion

We presented SPORE, a novel model checking algorithm that combines DPOR with symmetry reduction, and also exploits internal symmetries of C/C++ concurrent data structures. Our experiments confirm that SPORE outperforms the state-of-the-art by a wide margin.

There are several ways this work could be extended. First, we would like to see whether SPORE can handle other classes of programs in related domains, namely distributed algorithms and/or persistent programs, where similar symmetries appear. It remains to be seen whether those patterns exhibit symmetries that can be exploited in a similar fashion to enhance the applicability of automated verification techniques in those domains. Second, it would also be interesting whether SPORE can be applied to models like ARMv8 [Flur et al. 2016] and POWER [Alglave et al. 2014] that do allow TRUST’s `po ∪ rrf` cycles in consistent executions (which SPORE does not currently produce). Finally, SPORE could also be combined with testing techniques, so that only representative executions are produced when obtaining traces of a concurrent program.

## Acknowledgments

We thank the anonymous reviewers for their valuable feedback. This work was supported by a European Research Council (ERC) Consolidator Grant for the project “PERSIST” under the European Union’s Horizon 2020 research and innovation programme (grant agreement No. 101003349).

## Data-Availability Statement

The benchmarks and tools used to produce the results of this paper can be found at [Kokologiannakis et al. 2024a]. SPORE is available at [Kokologiannakis n.d.].

## References

- Parosh Aziz Abdulla, Stavros Aronis, Mohamed Faouzi Atig, Bengt Jonsson, Carl Leonardsson, and Konstantinos Sagonas. 2015. “Stateless model checking for TSO and PSO.” In: *TACAS 2015* (LNCS). Vol. 9035. Springer, Berlin, Heidelberg, 353–367. [https://doi.org/10.1007/978-3-662-46681-0\\_28](https://doi.org/10.1007/978-3-662-46681-0_28).
- Parosh Aziz Abdulla, Stavros Aronis, Bengt Jonsson, and Konstantinos Sagonas. 2014. “Optimal dynamic partial order reduction.” In: *POPL 2014*. ACM, New York, NY, USA, 373–384. <https://doi.org/10.1145/2535838.2535845>.

- Parosh Aziz Abdulla, Stavros Aronis, Bengt Jonsson, and Konstantinos Sagonas. Sept. 2017. "Source sets: A foundation for optimal dynamic partial order reduction." *J. ACM*, 64, 4, (Sept. 2017), 25:1–25:49. <https://doi.org/10.1145/3073408>.
- Parosh Aziz Abdulla, Mohamed Faouzi Atig, Bengt Jonsson, Magnus Lång, Tuan Phong Ngo, and Konstantinos Sagonas. Oct. 10, 2019. "Optimal stateless model checking for reads-from equivalence under sequential consistency." *Proc. ACM Program. Lang.*, 3, (Oct. 10, 2019), 150:1–150:29, OOPSLA, (Oct. 10, 2019). <https://doi.org/10.1145/3360576>.
- Parosh Aziz Abdulla, Mohamed Faouzi Atig, Bengt Jonsson, and Tuan Phong Ngo. Oct. 2018. "Optimal stateless model checking under the release-acquire semantics." *Proc. ACM Program. Lang.*, 2, OOPSLA, (Oct. 2018), 135:1–135:29. <https://doi.org/10.1145/3276505>.
- Elvira Albert, Miguel Gómez-Zamalloa, Miguel Isabel, and Albert Rubio. 2018. "Constrained dynamic partial order reduction." In: *CAV 2018*. Ed. by Hana Chockler and Georg Weissenbacher. Springer International Publishing, Cham, 392–410. ISBN: 978-3-319-96142-2. [https://doi.org/10.1007/978-3-319-96142-2\\_24](https://doi.org/10.1007/978-3-319-96142-2_24).
- Jade Alglave, Luc Maranget, and Michael Tautschnig. July 2014. "Herding cats: Modelling, simulation, testing, and data mining for weak memory." *ACM Trans. Program. Syst.*, 36, 2, (July 2014), 7:1–7:74. <https://doi.org/10.1145/2627752>.
- Stavros Aronis, Bengt Jonsson, Magnus Lång, and Konstantinos Sagonas. 2018. "Optimal dynamic partial order reduction with observers." In: *TACAS 2018 (LNCS)*. Vol. 10806. Springer, 229–248. [https://doi.org/10.1007/978-3-319-89963-3\\_14](https://doi.org/10.1007/978-3-319-89963-3_14).
- Samy Al Bahra. N.d. *Concurrency Kit*. (). <https://github.com/concurrencykit/ck>.
- Marek Chalupa, Krishnendu Chatterjee, Andreas Pavlogiannis, Nishant Sinha, and Kapil Vaidya. Dec. 2017. "Data-centric dynamic partial order reduction." *Proc. ACM Program. Lang.*, 2, POPL, (Dec. 2017), 31:1–31:30. <https://doi.org/10.1145/3158119>.
- Krishnendu Chatterjee, Andreas Pavlogiannis, and Viktor Toman. Oct. 2019. "Value-Centric Dynamic Partial Order Reduction." *Proc. ACM Program. Lang.*, 3, OOPSLA, (Oct. 2019). <https://doi.org/10.1145/3360550>.
- Edmund M. Clarke, Somesh Jha, Reinhard Enders, and Thomas Filkorn. 1996. "Exploiting symmetry in temporal logic model checking." *Form. Meth. Syst. Des.*, 9, 1/2, 77–104. <https://doi.org/10.1007/BF00625969>.
- Edmund M. Clarke, Daniel Kroening, and Flavio Lerdia. 2004. "A tool for checking ANSI-C programs." In: *TACAS 2004 (LNCS)*. Vol. 2988. Springer, Berlin, Heidelberg, 168–176. [https://doi.org/10.1007/978-3-540-24730-2\\_15](https://doi.org/10.1007/978-3-540-24730-2_15).
- Dave Dice and Alex Kogan. 2019. "TWA – Ticket Locks Augmented with a Waiting Array." In: *Euro-Par 2019*. Springer-Verlag, Berlin, Heidelberg, 334–345. ISBN: 978-3-030-29399-4. [https://doi.org/10.1007/978-3-030-29400-7\\_24](https://doi.org/10.1007/978-3-030-29400-7_24).
- Simon Doherty, Lindsay Groves, Victor Luchangco, and Mark Moir. 2004. "Formal Verification of a Practical Lock-Free Queue Algorithm." In: *FORTE 2004 (LNCS)*. Ed. by David de Frutos-Escrig and Manuel Núñez. Vol. 3235. Springer, 97–114. [https://doi.org/10.1007/978-3-540-30232-2\\_7](https://doi.org/10.1007/978-3-540-30232-2_7).
- Tayfun Elmas, Shaz Qadeer, and Serdar Tasiran. 2009. "A calculus of atomic actions." In: *POPL 2009*. Ed. by Zhong Shao and Benjamin C. Pierce. ACM, 2–15. <https://doi.org/10.1145/1480881.1480885>.
- E. Allen Emerson and Thomas Wahl. 2005. "Dynamic Symmetry Reduction." In: *TACAS 2005 (LNCS)*. Ed. by Nicolas Halbwachs and Lenore D. Zuck. Vol. 3440. Springer, 382–396. [https://doi.org/10.1007/978-3-540-31980-1\\_25](https://doi.org/10.1007/978-3-540-31980-1_25).
- Facebook. N.d. *Folly: Facebook Open-source Library*. (). <https://github.com/facebook/folly>.
- Cormac Flanagan, Stephen N. Freund, and Shaz Qadeer. 2005. "Exploiting Purity for Atomicity." *IEEE Trans. Software Eng.*, 31, 4, 275–291. <https://doi.org/10.1109/TSE.2005.47>.
- Cormac Flanagan and Patrice Godefroid. 2005. "Dynamic partial-order reduction for model checking software." In: *POPL 2005*. ACM, New York, NY, USA, 110–121. <https://doi.org/10.1145/1040305.1040315>.
- Shaked Flur, Kathryn E. Gray, Christopher Pulte, Susmit Sarkar, Ali Sezgin, Luc Maranget, Will Deacon, and Peter Sewell. 2016. "Modelling the ARMv8 architecture, operationally: Concurrency and ISA." In: *POPL 2016*. ACM, St. Petersburg, FL, USA, 608–621. ISBN: 978-1-4503-3549-2. <https://doi.org/10.1145/2837614.2837615>.
- Dominique Fober, Yann Orlarey, and Stéphane Letz. 2001. *Optimised Lock-Free FIFO Queue*. Technical Report. GRAME. <https://hal.archives-ouvertes.fr/hal-02158792>.
- Natalia Gavrilenko, Hernán Ponce-de-León, Florian Furbach, Keijo Heljanko, and Roland Meyer. 2019. "BMC for weak memory models: Relation analysis for compact SMT encodings." In: *CAV 2019*. Ed. by Isil Dillig and Serdar Tasiran. Springer International Publishing, Cham, 355–365. ISBN: 978-3-030-25540-4. [https://doi.org/10.1007/978-3-030-25540-4\\_19](https://doi.org/10.1007/978-3-030-25540-4_19).
- Michalis Kokologiannakis. N.d. *GenMC: Generic model checking for C programs*. (). <https://github.com/MPI-SWS/genmc>.
- Patrice Godefroid. 1997. "Model checking for programming languages using VeriSoft." In: *POPL 1997*. ACM, Paris, France, 174–186. <https://doi.org/10.1145/263699.263717>.
- Timothy L. Harris, Keir Fraser, and Ian A. Pratt. 2002. "A Practical Multi-word Compare-and-Swap Operation." In: *DISC 2002 (LNCS)*. Ed. by Dahlia Malkhi. Vol. 2508. Springer, 265–279. [https://doi.org/10.1007/3-540-36108-1\\_18](https://doi.org/10.1007/3-540-36108-1_18).
- Maurice Herlihy. 1991. "Wait-Free Synchronization." *ACM Trans. Program. Lang. Syst.*, 13, 1, 124–149.
- Maurice Herlihy and Nir Shavit. 2008. *The art of multiprocessor programming*.
- Max Khzhinsky. N.d. *CDS C++ library*. (). <https://github.com/khizmax/libcds>.

- Michalis Kokologiannakis, Ori Lahav, Konstantinos Sagonas, and Viktor Vafeiadis. Dec. 2017. “Effective stateless model checking for C/C++ concurrency.” *Proc. ACM Program. Lang.*, 2, POPL, (Dec. 2017), 17:1–17:32. <https://doi.org/10.1145/3158105>.
- Michalis Kokologiannakis, Iason Marmanis, Vladimir Gladstein, and Viktor Vafeiadis. Jan. 2022. “Truly stateless, optimal dynamic partial order reduction.” *Proc. ACM Program. Lang.*, 6, POPL, (Jan. 2022). <https://doi.org/10.1145/3498711>.
- Michalis Kokologiannakis, Iason Marmanis, and Viktor Vafeiadis. June 2024a. *SPORE: Combining Symmetry and Partial Order Reduction (Replication Package)*. (June 2024). <https://doi.org/10.5281/zenodo.10798179>.
- Michalis Kokologiannakis, Iason Marmanis, and Viktor Vafeiadis. June 2024b. “Spore: Combining Symmetry and Partial Order Reduction (supplementary material),” (June 2024). <https://plv.mpi-sws.org/genmc>.
- Michalis Kokologiannakis, Iason Marmanis, and Viktor Vafeiadis. 2023. “Unblocking Dynamic Partial Order Reduction.” In: *CAV 2023*. Vol. 13964. Springer, 230–250. [https://doi.org/10.1007/978-3-031-37706-8\\_12](https://doi.org/10.1007/978-3-031-37706-8_12).
- Michalis Kokologiannakis, Azalea Raad, and Viktor Vafeiadis. Oct. 2019a. “Effective lock handling in stateless model checking.” *Proc. ACM Program. Lang.*, 3, OOPSLA, (Oct. 2019). <https://doi.org/10.1145/3360599>.
- Michalis Kokologiannakis, Azalea Raad, and Viktor Vafeiadis. 2019b. “Model checking for weakly consistent libraries.” In: *PLDI 2019*. ACM, New York, NY, USA. <https://doi.org/10.1145/3314221.3314609>.
- Michalis Kokologiannakis, Xiaowei Ren, and Viktor Vafeiadis. 2021. “Dynamic Partial Order Reductions for Spinlocks.” In: *FMCAD 2021*. IEEE, 163–172. [https://doi.org/10.34727/2021/isbn.978-3-85448-046-4\\_25](https://doi.org/10.34727/2021/isbn.978-3-85448-046-4_25).
- Ori Lahav, Nick Giannarakis, and Viktor Vafeiadis. 2016. “Taming Release-acquire Consistency.” In: *POPL 2016*. ACM, St. Petersburg, FL, USA, 649–662. ISBN: 978-1-4503-3549-2. <https://doi.org/10.1145/2837614.2837643>.
- Ori Lahav, Viktor Vafeiadis, Jeehoon Kang, Chung-Kil Hur, and Derek Dreyer. 2017. “Repairing sequential consistency in C/C++11.” In: *PLDI 2017*. ACM, Barcelona, Spain, 618–632. ISBN: 978-1-4503-4988-8. <https://doi.org/10.1145/3062341.3062352>.
- Leslie Lamport. Sept. 1979. “How to Make a Multiprocessor Computer that Correctly Executes Multiprocess Programs.” *IEEE Trans. Computers*, 28, 9, (Sept. 1979), 690–691. <https://doi.org/10.1109/TC.1979.1675439>.
- Maged M. Michael and Michael L. Scott. 1998. “Nonblocking algorithms and preemption-safe locking on multiprogrammed shared memory multiprocessors.” *J. Parallel Distrib. Comput.*, 51, 1, 1–26.
- Huyen T. T. Nguyen, César Rodríguez, Marcelo Sousa, Camille Coti, and Laure Petrucci. 2018. “Quasi-optimal partial order reduction.” In: *CAV 2018 (LNCS)*. Ed. by Hana Chockler and Georg Weissenbacher. Vol. 10982. Springer, 354–371. [https://doi.org/10.1007/978-3-319-96142-2\\_22](https://doi.org/10.1007/978-3-319-96142-2_22).
- Brian Norris and Brian Demsky. 2013. “CDSChecker: Checking concurrent data structures written with C/C++ atomics.” In: *OOPSLA 2013*. ACM, 131–150. <https://doi.org/10.1145/2509136.2509514>.
- César Rodríguez, Marcelo Sousa, Subodh Sharma, and Daniel Kroening. 2015. “Unfolding-based Partial Order Reduction.” In: *CONCUR 2015 (LIPIcs)*. Vol. 42. Schloss Dagstuhl - Leibniz-Zentrum fuer Informatik, 456–469. <https://doi.org/10.4230/LIPIcs.CONCUR.2015.456>.
- SPARC International Inc.. 1994. *The SPARC architecture manual (version 9)*. Prentice-Hall.
- R. Kent Treiber. 1986. *Systems Programming: Coping with Parallelism*. Tech. rep. Technical Report RJ5118, IBM. <https://dominoweb.draco.res.ibm.com/58319a2ed2b1078985257003004617ef.html>.
- Thomas Wahl and Alastair Donaldson. 2010. “Replication and Abstraction: Symmetry in Automated Formal Verification.” 2, 799–847. <https://doi.org/10.3390/sym2020799>.

## A Formal Model

In this section, we define a simple programming language (§A.1), and show how programs in the language are mapped to execution graphs (§A.2).

### A.1 Programming Language

For the purposes of this paper, we introduce a simple imperative programming language with a top-level parallel composition. *Commands*,  $c \in \text{Cmd}$ , are given by the following grammar:

$$c ::= r := e \mid \mathbf{error} \mid \mathbf{block} \mid \mathbf{if} \ e \ \mathbf{then} \ c \mid c_1; c_2 \mid f^{annot}(e_1, \dots, e_n) \\ | r := \mathbf{load}^{o,k}(e) \mid \mathbf{store}^{o,k}(e_1, e_2) \mid r := \mathbf{alloc}() \mid \mathbf{free}(e)$$

where  $r \in \text{Reg}$  ranges over *registers*,  $f \in \text{Fname}$  over *function names*,  $annot \in \text{Annot} \triangleq \{\text{main}, \text{help}\}$  over *function annotations*,  $o \in \{\text{na}, \text{rlx}, \text{acq}, \text{rel}, \text{acqrel}, \text{sc}\}$  over RC11 *access modes* [Lahav et al. 2017],  $k \subseteq \{\text{excl}\}$  over sets of *attributes*, and  $e \in \text{Exp}$  over simple *expressions* built from integers  $n$ , registers, and arithmetic operators:

$$e ::= n \mid r \mid e_1 + e_2 \mid e_1 - e_2 \mid \dots$$

RC11 access modes are naturally ordered from weakest to strongest as follows:

$$\begin{array}{ccccccc} & & & \text{(acquire)} & & & \\ & & & \text{acq} & & & \\ & \text{na} & \sqsubset & & \sqsupset & \text{acqrel} & \sqsubset \text{sc} \\ \text{(non-atomic)} & & \text{rlx} & \text{(relaxed)} & & & \text{(seq.consistent)} \\ & & & \text{rel} & & & \\ & & & \text{(release)} & & & \end{array}$$

The only attribute we have for accesses is exclusivity flag `excl` used to denote when an access is part of a read-modify-write (RMW) instruction.

*Remark 3.* The primitive commands **error** and **block** commands can be used to model `assert` and `assume` statements as follows:

$$\mathbf{assert}(e) \triangleq \mathbf{if} \ \neg e \ \mathbf{then} \ \mathbf{error} \qquad \mathbf{assume}(e) \triangleq \mathbf{if} \ \neg e \ \mathbf{then} \ \mathbf{block}$$

*Remark 4.* For simplicity, we only allow function calls for the purpose of specifying internal symmetries. Thus, all function calls are annotated and do not return any results.

*Remark 5.* Commands do not contain any loops, since SMC only works for programs that are guaranteed to terminate. Programs with loops that are guaranteed to terminate in at most  $k$  iterations can be rewritten by unfolding those loops  $k$  times. Spinloops (even if non-terminating) can soundly be unrolled to a single iteration [Kokologiannakis et al. 2021], e.g., `do r := load(x) while(e)` is converted to `r := load(x); assume(¬e)`.

A *function definition* has the form  $f(r_1, \dots, r_n) \{ \mathbf{local} \ r_{n+1}, \dots, r_{n+m}; \ c_{body} \}$ , where  $f$  is the function name,  $r_1, \dots, r_n$  are the formal parameters,  $r_{n+1}, \dots, r_{n+m}$  are the local variables, and  $c_{body}$  is the function body. We assume that registers used in  $c_{body}$  belong to the function parameters or the declared local variables. For simplicity, we only allow function definitions that satisfy our internal symmetry constraints: the functions do not return any results, and their bodies comprise of a possibly empty sequence of loads followed by a compare-and-swap (CAS) on a location and with an expected value that does not depend on the prior loads, i.e. each  $c_{body}$  is of following form:

$$r_1 := \mathbf{load}(e_1); \dots; r_k := \mathbf{load}(e_k); r_0 := \mathbf{load}^{\text{excl}}(e_{loc}); \mathbf{if} \ r_0 = e_{exp} \ \mathbf{then} \ \mathbf{store}^{\text{excl}}(e_{loc}, e')$$

where  $k \geq 0$  and  $e_{loc}$  and  $e_{exp}$  do not depend on the registers  $r_0, \dots, r_k$ .



The simplest—and most common—kind of annotatable function is CAS-noret, which performs a CAS without returning whether it was successful.

$$\text{CAS-noret}(loc, exp, new) \{ \mathbf{local} \ r; \left( r := \mathbf{load}^{\text{excl}}(loc); \mathbf{if} \ r = exp \ \mathbf{then} \ \mathbf{store}^{\text{excl}}(loc, new) \right) \}$$

A program  $P \in \text{Prog}$  comprises a sequence of function definitions and a top-level parallel composition of commands  $c_1 \parallel \dots \parallel c_k$ . We assume that all function calls both in the parallel composition and in the function definitions themselves are to previously defined functions (so, in particular, no recursion is allowed) and that the number of arguments matches the number of formal parameters in the function's definition.

## A.2 Mapping Programs to Execution Graphs

Commands in our language are interpreted with respect to a *thread identifier*  $t \in \text{Tid} \triangleq \mathbb{N}$ , a *serial number*  $i \in \text{Idx} \triangleq \mathbb{N}$ , and an *environment*  $\Gamma \in \text{Env} \triangleq (\text{Reg} \rightarrow \text{Val}) \times (\text{Fname} \rightarrow (\text{Reg}^* \times \text{Cmd}))$ , mapping registers to values and function names to their definitions. We extend the domain of  $\Gamma$  to expressions  $e$  in the expected way; e.g.,  $\Gamma(e_1 + e_2) = \Gamma(e_1) + \Gamma(e_2)$ .

The interpretation of a command  $\llbracket c \rrbracket(t, i, \Gamma)$  yields a set of pairs of the form  $\langle o, E \rangle$ , where  $o$  denotes the command outcome, and  $E \in \text{Pexec} \triangleq \mathcal{P}(\text{Event})$  denotes the plain execution graph (i.e., the set of events) leading to  $o$ . The outcome  $o$  may in turn be either  $\perp$  (when the computation has not terminated successfully) or an updated serial number  $i'$  along with a new environment  $\Gamma'$ .

The interpretation function  $\llbracket \cdot \rrbracket : \text{Cmd} \rightarrow (\text{Tid} \times \text{Idx} \times \text{Env}) \rightarrow \mathcal{P}((\text{Idx} \times \text{Env})_{\perp} \times \text{Pexec})$  for commands is defined by induction over the command syntax.

We start with the base cases, which are straightforward.

$$\begin{aligned} \llbracket r := e \rrbracket(t, i, \Gamma) &\triangleq \{ \langle (i, \Gamma[r \mapsto \Gamma(e)]), \emptyset \rangle \} \\ \llbracket \mathbf{block} \rrbracket(t, i, \Gamma) &\triangleq \{ \langle \perp, \{ \langle t, i, B \rangle \} \rangle \} \\ \llbracket \mathbf{error} \rrbracket(t, i, \Gamma) &\triangleq \{ \langle \perp, \{ \langle t, i, \text{Error} \rangle \} \rangle \} \\ \llbracket \mathbf{store}^{o,k}(e_1, e_2) \rrbracket(t, i, \Gamma) &\triangleq \{ \langle (i+1, \Gamma), \{ \langle t, i, W^{o,k}(\Gamma(e_1), \Gamma(e_2)) \rangle \} \rangle \} \\ \llbracket r := \mathbf{load}^{o,k}(e) \rrbracket(t, i, \Gamma) &\triangleq \{ \langle (i+1, \Gamma[r \mapsto v]), \{ \langle t, i, R^{o,k}(\Gamma(e), v) \rangle \} \rangle \mid v \in \text{Val} \} \\ \llbracket r := \mathbf{alloc}() \rrbracket(t, i, \Gamma) &\triangleq \{ \langle (i+1, \Gamma[r \mapsto v]), \{ \langle t, i, A(v) \rangle \} \rangle \mid v \in \text{Val} \} \\ \llbracket \mathbf{free}(e) \rrbracket(t, i, \Gamma) &\triangleq \{ \langle (i+1, \Gamma), \{ \langle t, i, D(\Gamma(e)) \rangle \} \rangle \} \end{aligned}$$

An assignment yields the singleton set with an updated environment and no events. **block** and **error** yield  $\perp$  and a single block event or error event respectively. Stores and deallocations generate a single event, they increment the serial number to account for the generated event, and keep the environment intact. Loads and allocations return a graph with a new event for an arbitrary return value  $v \in \text{Val}$  (corresponding to the value read and to the newly allocated memory address respectively), increment the serial number, and return an updated environment with the mapping  $r \mapsto v$ .

The interpretation of the inductive cases also proceeds as expected, despite it being a bit more complex. The interpretation of **if**  $e$  **then**  $c$  is determined by the value of  $\Gamma(e)$ , and either yields the interpretation of  $c$  or the empty graph.

$$\llbracket \mathbf{if} \ e \ \mathbf{then} \ c \rrbracket(t, i, \Gamma) \triangleq \text{if } \Gamma(e) \neq 0 \ \text{then } \llbracket c \rrbracket(t, i, \Gamma) \ \text{else } \{ \langle (i, \Gamma), \emptyset \rangle \}$$

The interpretation of  $c_1; c_2$  comprises two cases, depending on the outcome of  $c_1$ : if the computation  $\llbracket c_1 \rrbracket(\Gamma)$  terminates successfully, then the resulting outcome is that of  $c_2$  (i.e.,  $o_2$ ), taking the union

of the generated executions; otherwise, the interpretation yields  $\langle \perp, E_1 \rangle$ .

$$\llbracket c_1; c_2 \rrbracket(t, i, \Gamma) \triangleq \{ \langle o_2, E_1 \cup E_2 \rangle \mid \langle (i_1, \Gamma_1), E_1 \rangle \in \llbracket c_1 \rrbracket(t, i, \Gamma) \wedge \langle o_2, E_2 \rangle \in \llbracket c_2 \rrbracket(t, i_1, \Gamma_1) \} \\ \cup \{ \langle \perp, E_1 \rangle \mid \langle \perp, E_1 \rangle \in \llbracket c_1 \rrbracket(t, i, \Gamma) \}$$

Finally, function calls are interpreted by first generating a marker event for the function call and then looking up the function definition in the environment  $\Gamma$ , and interpreting its body in a new environment mapping only the parameter names to the values  $v_i = \Gamma(e_i)$  passed as arguments.

$$\llbracket f^{annot}(e_1, \dots, e_n) \rrbracket(t, i, \Gamma) \triangleq \{ \langle (i', \Gamma), \{ \langle t, i, M^{annot}(f, v_1, \dots, v_n) \rangle \} \cup E \rangle \mid \langle (i', \_), E \rangle \in \llbracket c \rrbracket(t, i+1, \Gamma') \} \\ \text{where } v_i = \Gamma(e_i) \text{ and } \Gamma(f) = \langle r_1, \dots, r_n, c \rangle \text{ and } \Gamma' = [r_1 \mapsto v_1, \dots, r_n \mapsto v_n]$$

Observe that the call itself keeps the caller's environment  $\Gamma$  intact, capturing the fact that any updates by the function body are to local variables of the callee and do not propagate to the caller.

Having interpreted commands, we can finally define the interpretation of a program,  $\llbracket P \rrbracket$ , as a set of execution graphs, whose events come from the interpretations of the individual threads in an environment  $\Gamma_0$  that maps all the defined function names to their definitions.

$$\left[ \begin{array}{l} f_1(\text{args}_1) \{ \mathbf{local} \ ls_1; \ body_1 \} \\ \vdots \\ f_k(\text{args}_k) \{ \mathbf{local} \ ls_k; \ body_k \} \\ (c_1 \parallel \dots \parallel c_n) \end{array} \right] \triangleq \left\{ \begin{array}{l} \text{let } \Gamma_0 = \left[ \begin{array}{l} f_1 \mapsto \langle \text{args}_1, \ body_1 \rangle, \dots, \\ f_k \mapsto \langle \text{args}_k, \ body_k \rangle \end{array} \right] \text{ in} \\ G \in \text{Exec} \left[ \begin{array}{l} \exists E_1, \dots, E_n. \\ (\forall i. \langle \_, E_i \rangle \in \llbracket c_i \rrbracket(i, 0, \Gamma_0)) \\ \wedge G.E = \{ \text{init} \} \cup E_1 \cup \dots \cup E_n \end{array} \right] \end{array} \right\}$$

We also define an interpretation function  $\llbracket \cdot \rrbracket^{Annot}$ , that avoids expanding function calls annotated with `help`. This is defined exactly as  $\llbracket \cdot \rrbracket$  except when applied to function calls annotated with “`help`”, in which case it returns only the function call marker event:

$$\llbracket f^{\text{help}}(e_1, \dots, e_n) \rrbracket^{Annot}(t, i, \Gamma) \triangleq \{ \langle (i+1, \Gamma), \{ \langle t, i, M^{\text{help}}(f, v_1, \dots, v_n) \rangle \} \rangle \}$$

In contrast, function calls annotated with “`main`” are properly expanded:

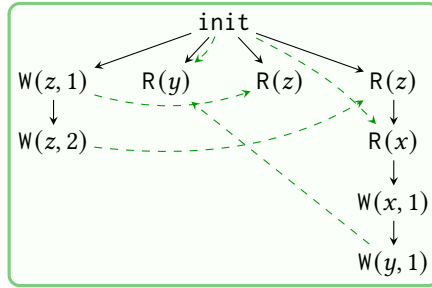
$$\llbracket f^{\text{main}}(e_1, \dots, e_n) \rrbracket^{Annot}(t, i, \Gamma) \triangleq \\ \{ \langle (i', \Gamma), \{ \langle t, i, M^{\text{main}}(f, v_1, \dots, v_n) \rangle \} \cup E \rangle \mid \langle (i', \_), E \rangle \in \llbracket c \rrbracket^{Annot}(t, i+1, \Gamma') \} \\ \text{where } v_i = \Gamma(e_i) \text{ and } \Gamma(f) = \langle r_1, \dots, r_n, c \rangle \text{ and } \Gamma' = [r_1 \mapsto v_1, \dots, r_n \mapsto v_n]$$

### B Changing Maximal Extensions for Symmetry Reduction

Modifying the revisiting condition of DPOR fails to restore completeness for Symmetry Reduction. To see why, consider the following program

$$\begin{array}{c}
 \text{T1: } z := 1 \\
 z := 2
 \end{array}
 \parallel
 \begin{array}{c}
 \text{T2: } a := y
 \end{array}
 \parallel
 \begin{array}{c}
 \text{T3: } r := z \\
 \text{if } (r \neq 1) \\
 \quad b := \text{CAS}(x, 0, 1) \\
 \quad \text{if } (b = 1) \\
 \quad \quad y := 1
 \end{array}
 \parallel
 \begin{array}{c}
 \text{T4: } r := z \\
 \text{if } (r \neq 1) \\
 \quad b := \text{CAS}(x, 0, 1) \\
 \quad \text{if } (b = 1) \\
 \quad \quad y := 1
 \end{array}
 \quad (\text{RMW-EXTENS})$$

where T3 and T4 are symmetric. The following execution is a consistent execution of **RMW-EXTENS** that satisfies our criterion for breaking symmetries (**IRREFLEXIVE**(**symb**; **eco**)).



We argue that this execution cannot be generated without changing the set of affected events by a revisit (i.e., by simply restricting the graph w.r.t. the **porf**-prefix of the revisitor).

To reach this execution, the write to *y* of T4 must revisit the read of T2, and thus the execution before the revisit must have T3 be maximally-extended with respect to the rest of the execution. After the read of *z* of T3 reads the maximal value (1), the succeeding RMW operation has no other consistent option but to read from the write to *y* of T4 (due to the atomicity constraint on RMW operations), but this forces the **eco** order to contradict the thread order. Therefore, the maximal-extension definition for this read cannot allow us to obtain the execution in question.

One possible solution to this problem might be to change the maximality condition of the reads that are **symb**-before some event in the **po**-prefix of the revisiting write, but this does not work for two reasons.

First, in case there are multiple such reads (e.g., if the symmetric threads of **RMW-EXTENS** also read a bunch of other variables before and after reading *z*, whose values are not used), which one should obey the non-standard maximality condition? How can we pick the “right” read?

Second, even if we somehow select the “right” read to change its maximality condition—or, say, we change the maximality condition for all reads that have the option of consistently reading from a **co**-earlier write—then reading from which write should be deemed the “maximal” one? Suppose that we add many other writes *z* := 3 to T1 of **RMW-EXTENS** before the *z* := 2 and both before and after *z* := 1. How would we pick the only “right” write event (namely, *W*(*x*, 1)) to deem it as the “maximal” one?

## C Helping Sufficient Conditions

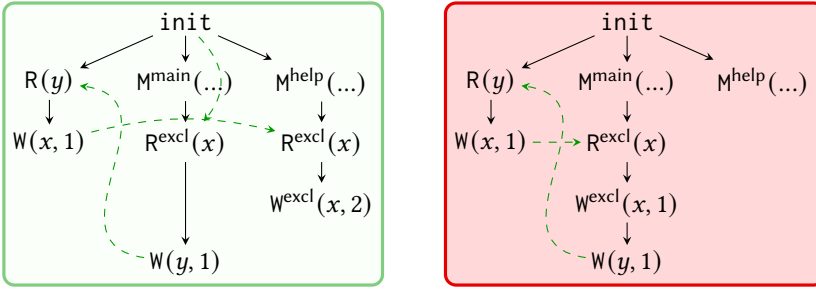
### C.1 Source Event

We present an example showing the importance of the source event being observed by the main thread. In the following program, both CASes can succeed by reading from the  $x := 1$  of  $T_1$ , which is, however, not observed before the main CAS.

$$T_1: r := y \quad \parallel \quad T_2: \boxed{\text{CAS}^{\text{main}}(x, 1, 2)} \quad \parallel \quad T_3: \boxed{\text{CAS}^{\text{help}}(x, 1, 2)} \quad (\text{NO-SOURCE-READ})$$

$$x := 1 \quad \parallel \quad y := 1$$

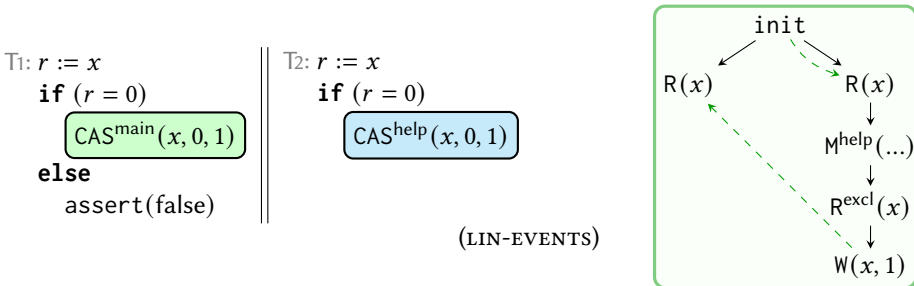
This creates a problem because  $T_1$  cannot read  $r = 1$  when the main CAS succeeds (due to the `porf`-cycle); yet  $T_1$  can read  $r = 1$  when the helping CAS succeeds, as shown in the execution graphs below.



Consequently, one cannot soundly eliminate the helping CAS in this case, and so we impose the condition that the source write must be observed by a thread before performing an operation that might be helped by other threads.

### C.2 Linearization Events

We present an example justifying why we need the immediate predecessor of the main function  $f_m$  to be observed before the helping function  $f_h$ . In the following program, this condition does not hold, and indeed the depicted execution, which reveals an error, would not be detected if we treated the helping function as a no-op. Our condition would avoid such scenarios by enforcing that, if there is no annotation error, any behavior in the main function happens independently (in a `porf` sense) of the helping function since execution are `porf` acyclic.



## D Completeness of Internal Symmetries

In this section, we instantiate the memory model  $M$  to RC11 [Lahav et al. 2017] with minor modifications. Below we provide the memory-model definition, as well as the corresponding annotation error definition.

### D.1 Memory Model

*Definition D.1 (Consistent Execution).* Given an execution  $G$ ,  $\text{consistent}_M(G)$  is the conjunction of the following predicates: (1)  $\text{porf}$  is irreflexive, (2)  $\text{hb}; \text{eco}$  is irreflexive, (3)  $\text{rmw} \cap (\text{rb}; \text{eco}) = \emptyset$ , and (4)  $\text{psc}$  is acyclic, where

- $\text{sw} \triangleq [E^{\exists \text{rel}}]; ([F]; \text{po})?; [W^{\exists \text{rlx}}]; (\text{rf}; \text{rmw})^*; \text{rf}; [R^{\exists \text{rlx}}]; (\text{po}; [F])?; [E^{\exists \text{acq}}]$
- $\text{hb} \triangleq (\text{po} \cup \text{sw})^+$
- $\text{psc} \triangleq [E^{\text{sc}}]; ([F]; \text{hb})?; (\text{hb})_{\text{loc}} \cup \text{coUrbUpoUpo}; \text{hb}; \text{po}; (\text{hb}; [F])?; [E^{\text{sc}}] \cup [F^{\text{sc}}]; \text{hb}; \text{eco}; \text{hb}; [F^{\text{sc}}]$

*Definition D.2 (Erroneous Execution).* Given an execution  $G$ ,  $\text{IsERRONEOUS}_M(G)$  is the disjunction of the following predicates:

- $G$  contains an explicit error event:  $G.\text{Error} \neq \emptyset$ .
- $G$  contains a memory access or deallocation event  $e$  to an unallocated memory address, i.e., where  $G$  either does not contain a  $A(\text{loc}(e))$  event, or where such an event exists but is not  $\text{hb}$ -before  $e$ .
- $G$  contains a *use-after-free* error, i.e., a deallocation event that is not  $\text{hb}$ -after all accesses to the deallocated location.
- $G$  contains more than one deallocation events to the same location.
- $G$  contains a *data race*, i.e., two  $\text{hb}$ -unordered accesses to the same location, at least one of which is a write, and at least one of which is “non-atomic”.

We lift  $\text{mod}(f_m)$  to return the successful access mode of the CAS instruction of  $f_m \in M^{\text{main}}$ .

### D.2 Annotation Error

*Definition D.3.* An event  $f_h \in M^{\text{help}}$  in an execution  $G$  is *matched*, if there exist (a) a corresponding  $f_m \in G.M^{\text{main}}$  with  $\text{arg}(f_m) = \text{arg}(f_h)$  and (b) a source write  $s \in G.W$  with  $\text{loc}(s) = \text{loc}(f_m)$  and  $\text{val}(s) = \text{exp}(f_m)$  (c) events  $l_w \in G.W^{\exists \text{rel}}$  and  $l_r \in G.R^{\exists \text{acq}}$  such that:

- $\langle s, f_m \rangle \in G.\text{rf}^?; [s']; \text{po}$
- $\langle f_m, f_h \rangle \in \text{po}^{-1}|_{\text{imm}}; [l_w]; G.\text{rf}; [l_r]; \text{po}$
- $\text{mod}(l_r) \not\subseteq \text{mod}(l_w)$

*Definition D.4 (Annotation error).* An execution  $G$  is *correctly annotated* if every  $f_h \in G.M^{\text{help}}$  is matched by an  $f_m \in G.M^{\text{main}}$  with a source write  $s$  such that for all  $w \in \text{rng}([s]; \text{co})$ ,  $w \in W^{\text{excl}}$  and  $\text{val}(w) \neq \text{val}(s)$ .

### D.3 Program Assumptions

We assume that every annotated function consists of an optional sequence of reads followed by a CAS instruction. We also assume that, if an annotated function includes a read instruction, then the successful access mode of the CAS instruction is  $\exists \text{acqrel}$ , and the failing access mode is  $\exists \text{acq}$ . Otherwise, i.e., if there are no read instructions in the annotated function, we require that the failed access mode of the CAS is at least as strong as the successful access mode of the CAS’s read. The reads have no external dependencies, apart from a possible data dependency to the write of the CAS instruction.

#### D.4 Completeness

The following lemma shows that we can remove the events of a helping function whose CAS instruction failed, while preserving both consistency and the presence of an error.

**LEMMA D.5.** *Let  $G$  be a consistent and erroneous execution and  $f_h \in \mathbb{M}^{\text{help}}$  a function call whose CAS instruction fails. Then, the execution that results from removing the events of  $f$  is also consistent and erroneous.*

**PROOF.** Since the CAS fails, all removed events are reads. Read events can only contribute to errors related to the lack of **hb** synchronization. Such errors, however, are also checked using the  $f_h$  event. Consistency is preserved by removing events.  $\square$

The following lemma presents the conditions under which we can replace the implementation of a main function (whose CAS instruction fails) with the implementation of a helping function whose CAS instruction succeeds and remove the helping function implementation events, while preserving consistency and the presence of an error.

**LEMMA D.6.** *Let  $G$  be a consistent and erroneous execution and  $f_h \in \mathbb{M}^{\text{help}}$ , such that  $G$  contains  $f_h$ 's implementation events. If  $f_h$ 's CAS  $r_h$  succeeds,  $f_h$  is matched by  $f_m \in \mathbb{M}^{\text{main}}$  with a source event  $s$ ,  $r_h$  reads from  $s$ , and  $f_m$  is either po-maximal or followed by a failed CAS  $r_m$  s.t.  $\langle r_h, r_m \rangle \in G.\text{rmw}; (G.\text{rf}; G.\text{rmw})^*; G.\text{rf}$ , then the execution where  $f_m$ 's implementation is replaced by  $f_h$ 's implementation, and  $f_h$ 's implementation is removed, is consistent and erroneous.*

**PROOF.** Let  $w_h$  be the CAS write of  $f_h$ . Since  $f_h$  is matched by  $f_m$ , there is a linearization write  $l_w$  po<sub>|imm</sub>-before  $f_m$  and a linearization read po-before  $f_h$ , such that  $\langle l_w, l_r \rangle \in G.\text{hb}$ . We reason about the resulting execution, by interpreting the transformation as if we replace the events of  $f_m$  with a dummy event, and swap the incoming and outgoing po edges of  $f_m$ 's and  $f_h$ 's events with each other. We write  $e_m$  to refer to  $r_m$  and the corresponding CAS write in  $G'$ . The helping CAS events ( $r_h$  and the following write) in  $G$  become  $e_m$  in  $G'$ .

By construction, the only possible additional edges in the resulting execution  $G'$  are po from and to events of  $G'.f_m$  (which were previously events of  $f_h$ ). Any  $G'.\text{po}$  edge to an event  $m$  of  $f_m$  (from an event not in  $f_m$ ) also exists as a po?;  $[l_w]; \text{hb}; [l_r]; \text{po}; [m]$  in  $G$ . Any  $G'.\text{po}$  edge from an event  $m$  of  $G'.f_m$  (to an event not in  $f_m$ , in which case  $f_m$  is not po-maximal) also exists as a  $[m]; \text{po?}; [r_h]; (\text{rf}; \text{rmw})^*; \text{rf}; [r_m]; \text{po}$  in  $G$ . Therefore, porf acyclicity is preserved. If the annotated functions contain read instructions, the aforementioned path from  $m$  is in **hb** (both CASes are at least acqrel), and therefore any additional po edge in  $G'$  is an **hb**; po edge in  $G$ . Otherwise,  $G'$  has additional **hb** edges that start with  $[e_m]; \text{po}$  (in which case  $f_m$  is not po-maximal in  $G$ ). Any **hb** edge that does not start with  $e_m$  also exists in  $G$ , since an po to  $e_m$  in  $G'$  is an po?; **hb**; po in  $G$  and an **sw** to  $e_m$  in  $G'$  is an **sw**;  $(\text{rf}; \text{rmw})^*; \text{rf} \subseteq \text{sw}$  in  $G$ .

Any **hb**-unordered error, i.e., error due to a lack of **hb** ordering between two events, is preserved since only **hb** edges originating from  $e_m$  are added in  $G'$ . To see this, consider such an error between two (different) events  $a$  and  $b$  of  $G$ . If none of the events are the helping CAS, then the events remain **hb**-unordered in  $G'$  (only **hb** edges from  $e_m$ , which is equivalent to the helping CAS in  $G$ , are added). Otherwise, if one of them is the helping CAS, then the error remains since events in  $\mathbb{M}^{\text{help}}$  are explicitly checked for **hb**-unordered errors. Additionally, the transformation does not remove any write events, and it therefore preserves possible annotation errors.

To see that  $G'.\text{psc}$  is acyclic, we will show that any **psc** cycle would also exist in  $G$ . First, we consider additional **psc** edges due to the added po that ends in  $e_m$ . We have shown that any po;  $[e_m]$  edge in  $G'$  is an po?; **hb**; po;  $[e_m]$  edge in  $G$ . The only interesting case is when the po;  $[e_m]$  edge is po<sub>|imm</sub>, i.e., starts with  $l_w$  (in every other case, replacing po with po; **hb**; po preserves the **psc**). In

this case, however, the  $[E^{sc}]; ([F]; hb)?; [l_w]; po|_{imm}; [e_m]; \dots$  edge in  $G'$  is in  $psc^2$  in  $G$ , using the  $[W^{sc}]; sw; [R^{sc}]$  edge from  $l_w$  to  $l_r$ . Therefore, no  $psc$  edge can be added due to the  $po; [e_m]$  edge.

Second, we consider which additional  $psc$  edges can exist due to the added  $po$  edges that start from  $e_m$  in  $G'$  (in which case  $f_m$  is not  $po$ -maximal in  $G$ ). Observe that the edges in  $hb|_{loc}$  that start with  $po$  and cannot be written as  $po \cup po; hb; po$  are of the form  $(po; hb?; sw)|_{loc}$ . The only additional  $psc$  edge are thus in one of the following forms

- (1)  $[E^{sc}]; ([F]; hb)?; (po; hb; [e_m]; po); (hb; [F])?; [E^{sc}]$
- (2)  $[E^{sc}]; ([F]; hb)?; ((po; hb?; sw)|_{loc} \cup po \cup po; hb; po); [e_m]; (po; hb?; [F]); [E^{sc}]$
- (3)  $[E^{sc}]; ([F]; hb)?; [e_m]; ((po; hb?; sw)|_{loc} \cup po \cup po; hb; po); (hb; [F])?; [E^{sc}]$

It is easy to see that in the first two cases, the same edge exists in  $G$ : any  $[e_m]; po$  part of the edge is preceded by a  $po \cup hb \cup sw$  edge, and thus the same path exists via the  $r_m$  event in  $G$ .

In the last case, if the  $psc$  edge starts with  $[F]; hb; [e_m]$ , then it also exists in  $G$  for the same reason (there is an  $hb$  to  $r_m$  in  $G$ ). Therefore, only  $psc$  edges of the form  $[e_m]; ((po; hb?; sw)|_{loc} \cup po \cup po; hb; po); (hb; [F])?; [E^{sc}]$ , can be added. In any  $psc$  cycle in  $G'$ , the  $psc; [e_m]$  edge ends in  $sw \cup po \cup co \cup rb$ . In every case, the same edge exists to  $r_m$ , and therefore the same cycle appears in  $G$  (any  $po$  edge from  $e_m$  in  $G'$  is a  $po$  edge from  $r_m$  in  $G$ ).  $\square$

Our completeness theorem states that if there is a consistent and erroneous execution under the original semantics, then there is a consistent and erroneous execution under the annotated semantics.

**THEOREM D.7.** *Let  $G \in \llbracket P \rrbracket_M$  such that  $ISERRONEOUS_M(G)$ . Then, there exists  $G' \in \llbracket P \rrbracket_M^{Annot}$  such that  $ISERRONEOUS_{SYM}(G)$ .*

**PROOF.** Let  $G$  be an erroneous execution of  $\llbracket P \rrbracket_M$  with the minimal number of helping function implementation events (such an execution exists from the hypothesis). If  $G$  contains no events corresponding to the implementation of a helping function, then the result follows immediately ( $G \in \llbracket P \rrbracket_M^{Annot}$ ). Otherwise, we will show that there exists a (not necessarily full) consistent and erroneous execution with at least one less helping function implementation. We can then maximally extend this execution (without adding implementation events of helping functions), and obtain a contradiction from the assumption about  $G$ .

Let  $f_h \in G.M^{help}$  that has implementation events. If the CAS of  $f_h$  is failing, from Lemma D.5 we obtain a full, consistent, and erroneous execution without  $f_h$ 's implementation events. Otherwise, the CAS of  $f_h$  succeeds. If  $f_h$  is not matched, we restrict  $G$  to the  $porf?$ -prefix of  $f_h$ . The resulting execution is erroneous and contains fewer helping function implementation events, concluding this case.

Otherwise, the CAS of  $f_h$  succeeds and  $f_h$  is matched by a  $f_m \in M^{main}$ . Let  $s_m$  be the source event of  $f_m$  and  $r_h$  the read of  $f_h$ 's CAS. If  $r_h$  is reading from  $w_d \neq s_m$ , then  $\langle s_m, w_d \rangle \in G.co$  due to coherence (since  $\langle s_m, f_h \rangle \in G.hb$ ). Restrict  $G$  to the  $porf$ -prefix of  $r_h$ . The resulting execution does not contain  $r_h$  (since  $G$  is  $porf$ -acyclic). Therefore we can remove the rest of  $f_h$ 's implementation events and obtain an execution with fewer helping function implementation events that is also erroneous: there is a write  $w_d \in rng([s_m]; co)$  that writes the expected value of  $f_h$ .

Otherwise, the CAS of  $f_h$  succeeds,  $f_h$  is matched by  $f_m \in M^{main}$ , and  $r_h$  is reading from  $s_m$ . If  $f_m$ 's CAS succeeds, the two CAS events cannot be reading from the same write (due to atomicity). So,  $f_m$  must be reading from some write  $w_1$  such that  $\langle s_m, w_1 \rangle \in G.co$  (due to coherence, since  $\langle s_m, f_m \rangle \in G.rf?; po$ ). Let  $w_m$  be the CAS write event of  $f_m$ 's implementation,  $w_h$  the CAS write event of  $f_h$ 's implementation, and let  $G'$  be the restriction of  $G$  to the set  $dom(G.porf?; [\{w_m, w_h\}])$ . It is easy to see that in  $G'$ , at least one of  $w_m, w_h$  are  $porf$ -maximal (because  $G$  is  $porf$ -acyclic), and there are at least two writes that write the expected value to the CAS location (the writes  $w_1$

and  $s_m$  that  $f_m$ 's and  $f_h$ 's CAS are reading, respectively). We consider two cases, depending on which one is `porf`-maximal. If  $w_h$  is `porf`-maximal we remove  $f_h$ 's implementation events. If  $w_m$  is `porf`-maximal we remove  $f_m$ 's implementation events and apply Lemma D.6 ( $f_m$  is `po`-maximal). In both cases, the resulting execution  $G''$  has fewer helping function implementation events and is erroneous:  $w_1, s_m, f_h \in G''.E$ .

Otherwise, the CAS of  $f_h$  succeeds,  $f_h$  is matched by  $f_m \in M^{\text{main}}$ ,  $r_h$  is reading from  $s_m$ , and  $f_m$ 's CAS fails. Let  $r_m$  the CAS read of  $f_m$ ,  $w_h$  the CAS write of  $f_h$ . If  $\langle w_h, r_m \rangle \in (G.\text{rf}; G.\text{rmw})^+; G.\text{rf}$ , we get a consistent and erroneous execution without  $f_h$ 's implementation events from Lemma D.6. Otherwise, there is a write event `co`-after  $w_h$  and `co?`; `rf`-before  $r_m$  that is not part of an RMW. Let  $w'$  be the `co`-latest such event. It is  $\langle w', r_m \rangle \in G.\text{porf}$ , and therefore  $\langle f_m, w' \rangle \notin G.\text{porf}$ . If  $\langle f_h, w' \rangle \in G.\text{porf}$ , we restrict  $G$  to the `porf?`-prefix of  $w'$  and  $f_m$ , in which  $f_m$  is `porf`-maximal, and apply Lemma D.6. Otherwise, we restrict to the `porf?`-prefix of  $w'$  and  $f_h$ , in which  $f_h$  is `porf`-maximal. In both cases, the resulting execution has fewer helping function implementation events and is erroneous (contains  $f_h$  and  $w'$ ), concluding the final case of our proof.  $\square$



## E Algorithm Correctness

In this section, we prove the correctness and optimality of our algorithm. The correctness is independent of the chosen memory model  $M$ , provided it satisfies some assumptions (§E.2).

In the sequel, we assume a program  $P$  s.t.  $\llbracket \llbracket M \rrbracket \rrbracket G$  only contains executions of finite size. Since  $\text{consistent}_{\text{SYM}}(G)$  is more restrictive than  $\text{consistent}_M(G)$ , the same holds for  $\llbracket \llbracket \text{SYM} \rrbracket \rrbracket G$ . We omit mentioning the program and the semantics when there is no ambiguity.

### E.1 Definitions

#### E.1.1 Preliminaries.

*Definition E.1 (Available).* The available set  $\text{avail}(G)$  of an execution  $G$  is the set of events that can extend the execution under the program semantics.

*Definition E.2 (Full Execution).* An execution  $G$  is full if it has no available events.

$$\text{full}(G) \triangleq \text{avail}(G) = \emptyset$$

*Definition E.3 (Open Read).* An event  $r \in R$  of an execution  $G$  is *open* if it is part of an RMW operation and there exists a matching write event in the available set of  $G$ .

$$\text{open}(G, r) \triangleq \exists w \in \text{avail}(G) \cap W. \langle r, w \rangle \in \text{rmw}$$

In the sequel, we lift  $G.\text{symbol}$  to also include the available events of the execution  $G$ .

*E.1.2 Operational steps.* Operational steps  $G \xrightarrow{e@e'} G'$  capture the non-revisit steps of the algorithm, namely that a graph  $G$  is extended by adding an extra event  $e$  that is  $G'.\text{cb}_{\text{SYM}}$ -maximal in the resulting graph  $G'$ . The event  $e'$  (if applicable) contains the extra information necessary to add  $e$  in a unique fashion (i.e., its  $\text{rf}$ -predecessor in the case of reads, and its  $\text{co}$ -predecessor in the case of writes).

$$\begin{array}{c} \text{READ} \\ r \in \text{avail}(G) \cap R \quad p \in G.W \quad \text{dom}(G.\text{symbol}; [r]) \in G.E \\ \hline \end{array}$$

$$G \xrightarrow{r@p} \text{AddRead}(G, r, p)$$

$$\begin{array}{c} \text{WRITE} \\ w \in \text{avail}(G) \cap W \quad p \in G.W \quad \text{dom}(G.\text{symbol}; [w]) \in G.E \\ \hline \end{array}$$

$$G \xrightarrow{w@p} \text{AddWrite}(G, w, p)$$

*Definition E.4 (Prefix).* Given executions  $G$  and  $G'$ ,  $G$  is a *prefix* of  $G'$ , if  $G$  can be extended to  $G'$  with a series of operational steps.

$$G \sqsubseteq G' \triangleq G \rightarrow^* G'$$

#### E.1.3 Maximal Steps.

*Definition E.5 (Maximal).* An event  $w \in W$  of an execution  $G$  is *maximal* if it has no  $\text{co}$  successor.

$$\text{ISMAXIMAL}(G, w) \triangleq \text{rng}([w]; G.\text{co}) = \emptyset$$

Maximal steps are those steps that add an event in  $\text{co}$ -maximal fashion, and thus allow the event to be affected by a revisit.

READ

$$\frac{r \in R \quad G \xrightarrow{r@p} G' \quad \text{IsMAXIMAL}(G, p)}{G \rightsquigarrow^r G'}$$

WRITE

$$\frac{\nexists r \in G.R. \text{ open}(G, r) \quad G \xrightarrow{w@p} G' \quad \text{IsMAXIMAL}(G, p)}{G \rightsquigarrow^w G'}$$

WRITE-EXCLUSIVE

$$\frac{w \in W \quad r \in R \quad \langle r, w \rangle \in \text{rmw} \quad \tilde{G} \rightsquigarrow^r G \xrightarrow{w@p} G' \quad \text{IsMAXIMAL}(G, p)}{G \rightsquigarrow^w G'}$$

*Definition E.6 (Maximal Completion).* Given an execution  $G$  and an event  $e$ ,  $\text{MAXCOMPLETION}(G, e)$  is the unique execution  $G'$  such that  $G \rightsquigarrow^e G'$ , if such an execution exists, and  $\perp$  otherwise.

We lift  $\text{MAXCOMPLETION}(G, \cdot)$  to sequences of events, with  $\text{MAXCOMPLETION}(\perp, \_) = \perp$ .

## E.2 Memory-Model

We assume an underlying memory model  $M$  with  $\text{cb}_M = (\text{po} \cup \text{rf})^+$ , whose consistency predicate  $\text{consistent}_M(\cdot)$  satisfies the following axioms.

**Axiom 1** ( $\text{cb}_M$  Acyclicity). *Given an execution  $G$ , if  $\text{consistent}_M(G)$ , then  $\text{ACYCLIC}(G, \text{cb}_M)$ .*

**Axiom 2** (Prefix Closedness). *Given an execution  $G$  and a set  $E \subseteq G.E$  such that  $\text{consistent}_M(G)$  and  $\text{dom}(G, \text{cb}_M; [E]) \subseteq E$ , it is  $\text{consistent}_M(G|_E)$ .*

**Axiom 3** (Extensibility). *Given an execution  $G$ , events  $e \in \text{avail}(G)$ ,  $w \in G.W$ , and an execution  $G'$  such that  $G \xrightarrow{e@w} G'$ ,  $\text{IsMAXIMAL}(G, w)$ , and  $\forall r \in G.R. \text{ open}(G, r) \Rightarrow \text{IsMAXIMAL}(G, G.\text{rf}(r))$ , if  $\text{consistent}_M(G)$ , then  $\text{consistent}_M(G')$ .*

We then define a new memory model  $\text{SYM}$ , with

$$\begin{aligned} \text{cb}_{\text{SYM}} &\triangleq (\text{po} \cup \text{rf} \cup \text{ymb})^+ \\ \text{consistent}_{\text{SYM}}(G) &\triangleq \text{consistent}_M(G) \wedge \text{IRREFLEXIVE}(\text{ymb}; \text{eco}) \end{aligned}$$

## E.3 Algorithm

*Definition E.7 (Configuration).* A configuration is a tuple  $\langle G, < \rangle$ , where  $G$  is an execution and  $<$  is a total order on  $G.E$ .

*Definition E.8 (Subsequence).* Given two sequences  $a$  and  $b$ ,  $a \sqsubseteq b$  stands for  $a$  being a subsequence of  $b$ .

We lift the notion of a prefix to configurations pointwise, i.e.,  $\langle G, < \rangle \sqsubseteq \langle G', <' \rangle$  if  $G \sqsubseteq G'$  and  $< \sqsubseteq <'$ , where the total orders are interpreted as the respective sequences.

Algorithmic steps  $\langle G, < \rangle \Rightarrow \langle G', <' \rangle$  occur whenever  $\text{EXPLORE}(G)$  calls  $\text{EXPLORE}(G')$  recursively: they capture the conditions that  $\text{EXPLORE}(G)$  checks and the computation it performs to calculate a  $G'$  in order to invoke itself recursively on  $G'$ .

NON-REVISIT STEP

$$\frac{e \in \text{avail}(G) \quad G \xrightarrow{e@p} G' \quad \text{consistent}_{\text{SYM}}(G')}{G \xrightarrow[\text{nr}]{e@p} G'}$$

WRITE REVISIT STEP

$$\frac{\begin{array}{l} w \in \text{avail}(G) \cap W \quad r \in G.R \\ P \triangleq \text{dom}((G \uplus \{w\}).\text{cb}_{\text{SYM}}; [\{w\}]) \quad r \notin P \\ [a_1, \dots, a_n] = \text{sort}_{<}(\{e \in G.E \setminus P \mid r \leq e\}) \end{array}}{G'' \xrightarrow{a_1} \dots \xrightarrow{a_n} G \quad G'' \xrightarrow{w@p} \xrightarrow{r@w} G' \quad \text{consistent}_{\text{SYM}}(G')} \\ \langle G, < \rangle \xrightarrow[\text{rv } r]{w@p} \langle G', \text{Restrict}(<, G''.E \cup \{r\}) \uparrow [w] \rangle$$

*Definition E.9 (Production Sequence).* A production sequence  $S$  is a sequence of algorithm steps that start from  $\langle G_0, \emptyset \rangle$  and  $\text{APPLY}(S)$  is the unique configuration obtained by applying all the steps of  $S$ .

We abuse notation and also write  $\text{APPLY}(S)$  for the projected execution of the configuration.

#### E.4 Lemmas and Propositions

**COROLLARY E.10 (UNIQUE EXTENSIBILITY).** *Given two execution such that  $G_0 \sqsubseteq G \rightsquigarrow G'$ , if  $\text{consistent}_{\text{SYM}}(G)$ , then  $\text{consistent}_{\text{SYM}}(G')$ .*

**PROOF.** From  $\text{consistent}_{\text{SYM}}(G)$ , we have  $\text{consistent}_{\text{M}}(G)$  and  $\text{IRREFLEXIVE}(G.\text{symp}; G.\text{eco})$ . From Axiom 3, it is  $\text{consistent}_{\text{M}}(G)$ . Since  $G_0 \sqsubseteq G$ , it is  $\text{dom}(G.\text{symp}; [G.E]) \subseteq G.E$ . Let  $e$  be the added event. By definition of  $\rightsquigarrow$ ,  $\text{rng}([e]; G'.\text{eco}) = \emptyset$ . Thus, any  $G'.\text{symp}; G'.\text{eco}$  loop must have a  $G'.\text{symp}$  edge that starts from  $e$ , contradicting  $\text{dom}(G.\text{symp}; [G.E]) \subseteq G.E$ . Therefore,  $\text{consistent}_{\text{SYM}}(G')$ .  $\square$

**COROLLARY E.11 (PREFIX CLOSEDNESS).** *Given two executions  $G$  and  $G'$  s.t.  $G \sqsubseteq G'$ , if  $\text{consistent}_{\text{SYM}}(G')$ , then  $\text{consistent}_{\text{SYM}}(G)$ .*

**PROOF.** From Axiom 2 and the fact that irreflexivity is prefix-closed.  $\square$

**PROPOSITION E.12.** *For any execution graph  $G, G_0 \sqsubseteq G$  iff  $\text{ACYCLIC}(G.\text{cb}_{\text{SYM}})$  and  $\text{dom}(G.\text{symp}; [G.E]) \subseteq G.E$ .*

**PROPOSITION E.13.** *For any execution graph  $G$  s.t.  $G_0 \Rightarrow^* G, G_0 \sqsubseteq G$ .*

**PROOF.** Proof by induction on the length of the production sequence. The non-revisit step case is trivial. For the revisit step  $G \xrightarrow[\text{rv } r]{w@p} G'$ , we have  $\text{dom}(G.\text{symp}; [w]) \subseteq G.E$ . For the execution  $G''$  after the removal of the affected events, we have  $G_0 \sqsubseteq G''$ , since  $G'' \rightsquigarrow^+ G$  (i.e., the maximal steps in  $G_0 \sqsubseteq G$  can commute to the end). Therefore, from the revisit condition  $G'' \rightarrow \rightarrow G'$ , we have  $G_0 \sqsubseteq G'$ .  $\square$

**PROPOSITION E.14.** *For any execution graph  $G$  s.t.  $G_0 \Rightarrow^* G, \text{dom}(G.\text{symp}; [\text{next}_P(G)]) \subseteq G.E$ .*

**PROOF.**  $\text{next}_P(\cdot)$  always picks the left-most available event  $e$ , and therefore there can be no event in  $\text{avail}(G)$  that is  $\text{symp}$ -before  $e$ .  $\square$

**PROPOSITION E.15.** *For any execution graph  $G$  s.t.  $G_0 \Rightarrow^* G, \text{ACYCLIC}(G.\text{cb}_{\text{SYM}})$  and  $\text{dom}(G.\text{cb}_{\text{SYM}}; [G.E]) \subseteq G.E$ .*

PROOF. Follows from Prop. E.13 and Prop. E.12.  $\square$

*Definition E.16.* Given a production sequence  $S$  that ends in  $G$ , i.e.,  $G = \text{APPLY}(S)$ , we define  $rv(S)$  as the subset of events that revisited in a revisit step of  $S$ , i.e.,  $rv(S) \triangleq \left\{ w \in W \mid \exists \xrightarrow[r]{w@-} \in S \right\}$ , and  $mrv(S)$  the subset of  $rv(S)$  such that the respective revisited read event was not later revisited or deleted in  $S$ , i.e.,

$$mrv(S) \triangleq \left\{ w \in W \mid \begin{array}{l} \exists S_r, t \in \xrightarrow[r]{w@-}. S_r \dashv\vdash t \sqsubseteq S \wedge \forall S', t'. \\ S_r \dashv\vdash t \sqsubseteq S' \dashv\vdash t' \sqsubseteq S \Rightarrow t' \notin \xrightarrow[r]{w@-} \wedge r \in \text{APPLY}(S' \dashv\vdash t'). \end{array} \right\}$$

LEMMA E.17. *Let  $S$  be a production sequence s.t.  $\langle G, \langle \rangle = \text{APPLY}(S)$ . If  $\langle G, \langle \rangle \xrightarrow[r]{w@-} \langle G', \langle \rangle$ , then  $[G.E]; G.\text{cb}_{\text{SYM}}?; [G'.E \setminus \{r\}] \subseteq [G'.E]; G'.\text{cb}_{\text{SYM}}?; [G'.E]$ .*

PROOF. By definition of the revisit step, all  $\text{po} \cup \text{rf} \cup \text{symp}$  edges ending in events that are not affected by the revisit, i.e., the revisited read and the deleted events, remain unaltered.  $\square$

LEMMA E.18. *Let  $S$  be a production sequence s.t.  $\langle G, \langle \rangle = \text{APPLY}(S)$ . If  $\langle G, \langle \rangle \xrightarrow[r]{w@-} \langle G', \langle \rangle$ , then  $mrv(S) \cap G.E \subseteq G'.E$ .*

PROOF. Let  $w' \in mrv(S) \cap G.E$  and assume that  $w' \notin G'.E$ . Since  $w'$  revisited a read  $r$  that was not revisited or deleted later in  $S$ , it must be  $\langle w', r \rangle \in G.\text{rf}$  and  $w' > r$ . For the revisit step from  $G$  to  $G'$ , we have that there is an execution  $G''$  such that  $G'' \rightsquigarrow^* G_1 \xrightarrow[w']{w'} G_2 \rightsquigarrow^* G$ . Because  $w' > r$ , it is  $\langle w', r \rangle \in G_2.\text{rf}$ , which contradicts  $G_1 \rightsquigarrow^* G_2$ .  $\square$

LEMMA E.19. *Let  $S$  be a production sequence s.t.  $\langle G, \langle \rangle = \text{APPLY}(S)$ . Then,  $rv(S) \subseteq \text{dom}([G.E]; G.\text{cb}_{\text{SYM}}?; [mrv(S)])$ .*

PROOF. Proof by induction on the length of the production sequence. For the empty sequence the result is trivial ( $rv(\emptyset) = \emptyset$ ). Let  $S$  be a production sequence, and  $S' = S \dashv\vdash t$ , i.e.,  $\langle G, \langle \rangle \Rightarrow \langle G', \langle \rangle$  where  $\langle G, \langle \rangle = \text{APPLY}(S)$  and  $\langle G', \langle \rangle = \text{APPLY}(S')$ . If  $t$  is a non-revisit step then the result is obvious since  $mrv(S) = mrv(S')$ ,  $rv(S) = rv(S')$ , and  $G.\text{cb}_{\text{SYM}} \subseteq G'.\text{cb}_{\text{SYM}}$ . Otherwise,  $t$  is a  $\xrightarrow[r]{w''@-}$  step.

Let  $w \in rv(S')$ . If  $w = w''$ , it is obvious that  $w \in \text{dom}([G'.E]; G'.\text{cb}_{\text{SYM}}?; [mrv(S')])$  ( $w'' \in mrv(S')$ ). Otherwise,  $w \in rv(S)$  ( $rv(S') = rv(S) \cup \{w''\}$ ). From the inductive hypothesis,  $rv(S) \subseteq \text{dom}([G.E]; G.\text{cb}_{\text{SYM}}?; [mrv(S)])$ . From Lemma E.18 and Lemma E.17,  $[G.E]; G.\text{cb}_{\text{SYM}}?; [mrv(S) \cap G.E] \subseteq [G'.E]; G'.\text{cb}_{\text{SYM}}?; [G'.E]$ . Since  $mrv(S) \subseteq rv(S)$  and  $rv(S) \subseteq G.E$ , it is  $mrv(S) \subseteq G.E$  and it suffices to show that  $mrv(S) \subseteq \text{dom}(G'.\text{cb}_{\text{SYM}}?; [mrv(S')])$ . Let  $w' \in mrv(S)$  and  $r$  the respective event that  $w'$  revisited. It is  $r < w'$  and  $\langle w', r \rangle \in G.\text{rf}$ . If  $r$  was not revisited or deleted by  $t$ , our result follows immediately ( $w' \in mrv(S')$ ). Otherwise,  $t$  revisited  $r'$  and revisited or deleted  $r \geq r'$ . From Lemma E.18,  $w' \in G'.E$ , and since  $w' > r'$ , it must be  $\langle w', w'' \rangle \in G'.\text{cb}_{\text{SYM}}$ , concluding our proof ( $w'' \in mrv(S')$ ).  $\square$

PROPOSITION E.20. *Let  $\langle G, \langle \rangle$  be a configuration s.t.  $\langle G_0, \emptyset \rangle \xrightarrow[r]{w@-} \langle G, \langle \rangle$ . There is no production sequence starting from  $\langle G, \langle \rangle$  that deletes  $w$ .*

PROOF. Follows directly from Lemma E.19 since in any later production sequence  $S$ ,  $w \in rv(S)$ .  $\square$

PROPOSITION E.21 (TERMINATION). *Any production sequence has finite length.*

PROOF. From Prop. E.20, any event that revisited cannot be deleted. Therefore, the lexicographical order  $\langle rv(S), \text{APPLY}(S).E \rangle$  increases with each algorithm step, and is bounded above since  $rv(S) \subseteq \text{APPLY}(S).E$  and the program semantics only contain executions of finite size.  $\square$

PROPOSITION E.22 (WELL-FORMEDNESS). *Given an execution  $G$  such that  $G_0 \Rightarrow^+ G$ ,  $G$  has at most one open read, and if it has an open read  $r \in G.R$ , then  $r$  was added or revisited in the last step.*

PROOF. Proof by induction on the length of the production sequence  $S$ . The base case where there is only one step in  $S$  is trivial (there can only be one event  $e$  that was added in the previous step). Let two executions such that  $G \Rightarrow G'$ , and  $t$  the corresponding step. If  $\text{next}_P(G) \notin W$ ,  $t$  is a non-revisit step and the result follows immediately: only  $\text{next}_P(G)$  can be open in  $G'$ , since  $G$  has at most one open read from the inductive hypothesis, which  $\text{next}_P(G)$  would pick. If  $t$  is a non-revisit step,  $G'$  has no open reads. Otherwise,  $t$  is a revisit step. Let  $r'$  the revisited read,  $\bar{G}$  the last execution in  $S$  before  $G$  where  $r'$  was added or last revisited. Additionally, let  $\bar{S} \sqsubseteq S$  the production sequence of  $\bar{G}$ . All events of  $\bar{G}$  are either  $\bar{\leq}$ -before  $r'$  or in the  $\text{cb}_{\text{SYM}}?$ -prefix of an event in  $mrv(\bar{S})$  (the write that revisited  $r'$  to reach  $\bar{G}$ ). From Prop. E.20, the latter events cannot be deleted. Additionally, no other event of  $\bar{G}$  can be revisited before  $t$ . Assume  $r'' \in \bar{G}.E$  is revisited by a write  $w''$ . It is  $r'' \bar{\leq} r'$ , and since  $r'$  is not revisited or deleted until  $t$ ,  $r'$  is in the  $\text{cb}_{\text{SYM}}?$ -prefix of  $w''$ . From Prop. E.20, this contradicts that  $t$  revisits  $r'$ : it would delete  $w''$  (Lemma E.17), but  $w''$  revisited earlier an event.

Since no event of  $\bar{G}$  is revisited until  $t$ , and only the events of  $\bar{G}$  that are  $\bar{\leq}$ -before  $r'$  can be deleted, it is  $\bar{G} \setminus \{r'\} \sqsubseteq G'$ . Additionally, all events in  $G'.E \setminus \bar{G}.E$  are in the  $\text{cb}_{\text{SYM}}?$ -prefix of a write, and therefore cannot contain an open read. Therefore, the only open read in  $G'$  can be  $r'$ , which was just revisited.  $\square$

PROPOSITION E.23. *Let two production sequences  $S$  and  $S'$  with  $S \sqsubset S'$ , and let  $\langle G, < \rangle \triangleq \text{APPLY}(S)$  and  $\langle G', <' \rangle \triangleq \text{APPLY}(S')$ . Then,  $G \sqsubseteq G'$  iff no step of  $S' \setminus S$  revisits an event of  $G$ . Additionally, if no step of  $S' \setminus S$  revisits an event of  $G$ , then  $< ++ \text{next}_P(G) \sqsubseteq <'$ .*

PROOF. We will first show the forward direction. Assume there is a step in  $S' \setminus S$  that revisits an event of  $G$  and let  $r$  be a  $<$ -minimal event such event of  $G.E$ , and  $t$  the first revisit of  $r$  in  $S' \setminus S$ . Let  $\langle G_1, <_1 \rangle$  and  $\langle G_2, <_2 \rangle$  the configurations before and after  $t$ , respectively, and  $w'$  be the event that revisits in  $t$ . It is easy to see that  $G.\text{rf}(r) = G_1.\text{rf}(r)$ , and therefore  $w \triangleq G.\text{rf}(r) \neq G_2.\text{rf}(r) = w'$ . From the revisit condition, it must be  $w <_1 r$  or  $\langle w, w' \rangle \in (G_1 \uplus \{w'\}).\text{cb}_{\text{SYM}}$  (and therefore  $w \in G_2.E$ ): in the other case,  $w$  would be in the deleted set and the maximality condition would fail. In either case, from Prop. E.20, no step of  $S'$  after  $G_2$  can delete  $w$ . Therefore, it cannot be that  $r$  reads from  $w$  in  $G'$ , contradicting  $G \sqsubseteq G'$ .

For the opposite direction, it is easy to see that if no event of  $G$  is revisited, it must be  $\langle G, < \rangle \sqsubset \langle G', <' \rangle$ , and since  $\text{next}_P(G)$  will be added in the first step of  $S' \setminus S$  and no earlier event is revisited, it is  $< ++ \text{next}_P(G) \sqsubseteq <'$ .  $\square$

LEMMA E.24 (PREFIX EXTENSION). *Given two executions  $G$  and  $G'$  s.t.  $G \sqsubset G'$ , and an event  $w \in G'.E \setminus G.E$ , there is a unique execution  $G_p$  s.t.  $G \sqsubseteq G_p \sqsubseteq G'$  and  $G_p.E \setminus G.E = \text{dom}(G'.\text{cb}_{\text{SYM}}; [\{w\}]) \setminus G.E$ . We call this execution the prefix-extension of  $G$  until  $w$  of  $G'$ , and denote it as  $\text{PREFIXEXTENSION}(G, G', w)$ .*

LEMMA E.25 (NEXT PREFIX). *Given two executions  $G_s$  and  $G_t$  s.t.  $G_s \sqsubset G_t$ , and an event  $e \in \text{avail}(G_s) \cap G_t.E$ , if there is no step s.t.  $G_s \xrightarrow{e@-} G' \sqsubseteq G_t$ , then  $e \in R$ ,  $w \triangleq G_t.\text{rf}(e) \notin G_s.W$ , and  $G_p \xrightarrow{w@p} \xrightarrow{e@w} G_c \sqsubseteq G_t$ , where  $G_p \triangleq \text{PREFIXEXTENSION}(G_s, G_t, w)$  and  $p \triangleq G_t|_{G_p.E \cup \{w\}}.\text{co}(w)$ . Additionally, for any execution  $G' \sqsupset G_s$  such that  $e \in G'.E$ , it is  $G_c \sqsubseteq G'$ .*

**Algorithm 2** Production sequence

---

```

1: procedure PRODUCTIONSEQUENCE( $G_f$ )
2:    $S \leftarrow \emptyset$ 
3:   while APPLY( $S$ )  $\neq G_f$  do
4:      $S \leftarrow \text{GETNEXT}(S, G_f)$ 
5:   return  $S$ 

6: procedure GETNEXT( $S_0, G_t$ )
7:    $G_{S_0} \leftarrow \text{APPLY}(S_0)$ 
8:    $e_0 \leftarrow \text{next}_p(G_{S_0})$ 
9:   if  $\exists p. G_{S_0} \xrightarrow{e_0 @ p} G' \wedge G' \sqsubseteq G_t$  then
10:    return  $S_0 \text{ ++ } \begin{matrix} e_0 @ p \\ \Rightarrow \\ nr \end{matrix}$ 
11:    $w \leftarrow G_t.\text{rf}(e_0)$ 
12:    $G_p \leftarrow \text{PREFIXEXTENSION}(G_{S_0}, G_t, w)$ 
13:    $p \leftarrow G_t|_{G_p.E \cup \{w\}}.\text{co}(w)$ 
14:    $\langle S, A \rangle \leftarrow \langle S_0, \emptyset \rangle$ 
15:   while true do
16:      $e \leftarrow \text{next}_p(\text{APPLY}(S))$ 
17:     if  $e = w$  then
18:       return  $S \text{ ++ } \begin{matrix} w @ p \\ \Rightarrow \\ rv \ e_0 \end{matrix}$ 
19:     if  $e \notin G_p.E$  then
20:        $A \leftarrow A \text{ ++ } e$ 
21:    $S \leftarrow \text{GETNEXT}(S, \text{MAXCOMPLETION}(G_p, A))$ 

```

---

**E.5 Completeness and Optimality**

LEMMA E.26. *Let  $S_0$  be a production sequence, and  $G_t$  an execution such that  $\text{consistent}_{\text{SYM}}(G_t)$ ,  $\text{APPLY}(S) \triangleq G_{S_0}$ ,  $G_0 \sqsubseteq G_{S_0} \sqsubset G_t$  and  $\text{next}_p(G_{S_0}) \in G_t.E$ . Then  $\text{GETNEXT}(S_0, G_t)$  returns a production sequence  $S' \sqsupset S$  such that  $G_{S_0} \sqsubset G' \sqsubseteq G_t$ , where  $G' = \text{APPLY}(S')$ . Additionally, for any production sequence  $\hat{S} \sqsupset S_0$  such that  $\text{APPLY}(\hat{S}) \sqsupseteq G_t$ , it is  $\hat{S} \sqsupseteq S'$ .*

PROOF SKETCH: By induction on the lexicographical order  $\langle -|G_{S_0}.E|, |G_t.E| \rangle$  of the arguments. Since the program semantics only contain executions of finite size and  $G_{S_0} \sqsubset G_t$ , the measure is bounded below.

LET:  $\langle G_{S_0}, <_{S_0} \rangle \triangleq \text{APPLY}(S_0)$

ASSUME: 1.  $G_0 \sqsubseteq G_{S_0} \sqsubset G_t$   
 2.  $\text{consistent}_{\text{SYM}}(G_t)$   
 3.  $\text{next}_p(G_{S_0}) \in G_t.E$

LET:  $S' \triangleq \text{GETNEXT}(S_0, G_t)$

PROVE: 1.  $S_0 \sqsubset S'$ ,  $\text{APPLY}(S') = \langle G', <' \rangle$ , and  $G_{S_0} \sqsubset G' \sqsubseteq G_t$   
 2.  $<_{S_0} \text{ ++ } \text{next}_p(G_{S_0}) \sqsubseteq <'$ ,  $\text{LAST}(S')$  either adds or revisits  $\text{next}_p(G_{S_0})$   
 3. If  $\hat{S} \sqsupset S_0$  and  $\text{APPLY}(\hat{S}) \sqsupseteq G_t$ , then  $\hat{S} \sqsupseteq S'$

$\langle 1 \rangle$ 1. SUFFICES: Prove  $\langle 0 \rangle$  under the assumption that it holds for any pair  $\langle S'_0, G'_t \rangle$  such that  $\langle -|\text{APPLY}(S'_0).E|, |G'_t.E| \rangle < M \triangleq \langle -|G_{S_0}.E|, |G_t.E| \rangle$ .

PROOF: Induction on the lexicographical order  $\langle - | \text{APPLY}(S_0).E |, | G_t.E | \rangle$  of the arguments  $\langle S_0, G_t \rangle$ . The order is bounded below because the program semantics only contain executions with finite size and  $G_{S_0} \sqsubset G_t$ .

$\langle 1 \rangle 2$ . CASE: The test in Line 9 succeeds.

$\langle 2 \rangle 1$ . Proof obligations 1 and 2 of  $\langle 0 \rangle$  hold.

PROOF: From §E.3 and  $\text{consistent}_{\text{SYM}}(G')$  ( $\text{consistent}_{\text{SYM}}(G_t)$  and Corollary E.11).

$\langle 2 \rangle 2$ . Proof obligation 3 holds.

$\langle 3 \rangle 1$ .  $p \in G_{S_0}.E \cup \{ \_ \}$

PROOF: From  $\langle 1 \rangle 2$ .

LET: Let  $t$  the step in Line 9

$\langle 3 \rangle 2$ . ASSUME:  $\hat{S} \sqsupseteq S \dashv\vdash t'$ , with  $t \neq t'$

PROVE: FALSE

$\langle 4 \rangle 1$ .  $S \sqsubset \hat{S}$  and  $\text{APPLY}(S) \sqsubseteq \text{APPLY}(\hat{S})$

$\langle 4 \rangle 2$ .  $\hat{S} \setminus S$  does not revisit an event of  $G_{S_0}.E$  and  $e_0 \in \text{APPLY}(\hat{S}).E$ .

PROOF: From  $\langle 4 \rangle 1$  and Prop. E.23.

$\langle 4 \rangle 3$ . Q.E.D.

PROOF: Contradiction from  $\langle 4 \rangle 2$ ,  $\langle 3 \rangle 1$  and  $t \neq t'$ :  $p \in G_{S_0}$  and it will not be deleted later, therefore  $e_0$  will always be in the wrong placement  $p'$  of  $t'$ .

$\langle 2 \rangle 3$ . Q.E.D.

$\langle 1 \rangle 3$ . CASE: The test in Line 9 fails.

$\langle 2 \rangle 1$ .  $e_0 \in R$  and  $G_t.\text{rf}(e_0) \notin G_{S_0}.W$

PROOF: From Lemma E.25.

$\langle 2 \rangle 2$ . LET: 1.  $w \triangleq G_t.\text{rf}(e_0)$

2.  $G_p \triangleq \text{PREFIXEXTENSION}(G_{S_0}, G_t, w)$

3.  $p \triangleq G_t |_{G_p.E \cup \{w\}}.\text{co}(w)$

$\langle 2 \rangle 3$ .  $\text{consistent}_{\text{SYM}}(G_p)$

PROOF: From  $\text{consistent}_{\text{SYM}}(G_t)$ ,  $G_p \sqsubseteq G_t$ , and Corollary E.11.

$\langle 2 \rangle 4$ .  $\text{ACYCLIC}(G_t.\text{cb}_{\text{SYM}})$

PROOF: From  $G_\emptyset \sqsubseteq G_t$  and Prop. E.12.

$\langle 2 \rangle 5$ . ASSUME:  $e_0 \in G_p.E$

PROVE: FALSE

$\langle 3 \rangle 1$ .  $\langle e_0, w \rangle \in G_t.\text{cb}_{\text{SYM}}$

PROOF: From  $\langle 2 \rangle 5$ , the definition of  $G_p$ , and  $e_0 \notin G_{S_0}.E$ .

$\langle 3 \rangle 2$ .  $\langle w, e_0 \rangle \in G_t.\text{rf}$

PROOF: By definition of  $w$ .

$\langle 3 \rangle 3$ . Q.E.D.

PROOF: Contradiction from  $\langle 3 \rangle 1$ ,  $\langle 3 \rangle 2$ , and  $\langle 2 \rangle 4$ .

$\langle 2 \rangle 6$ . ASSUME:  $\hat{S} \sqsupset S_0$  and  $\text{APPLY}(\hat{S}) \sqsupseteq G_t$

PROVE: There exist  $\bar{S}$ ,  $\bar{G}$ , and  $\bar{A}$  such that

1.  $p \triangleq G_t |_{G_p.E \cup \{w\}}.\text{co}(w)$

2.  $S_0 \sqsubset \bar{S} \dashv\vdash \xrightarrow[r \vee e_0]{w @ p} \hat{S}$

3.  $\text{APPLY}(S_0) \sqsubset \text{APPLY}(\bar{S}) = \langle \bar{G}, \bar{<} \rangle$

4.  $\bar{G} = \text{MAXCOMPLETION}(G_p, \bar{A})$

5.  $\bar{A} = \text{sort}_{<}(\bar{G}.E \setminus G_p.E)$

6.  $\text{next}_p(\bar{G}) = w$

$\langle 3 \rangle 1$ . There is no step in  $\hat{S} \setminus S_0$  that revisits an event of  $G$ .

PROOF: From Prop. E.23.

⟨3⟩2. Every configuration  $\langle G', <' \rangle$  in  $\hat{S} \setminus S_0$  after the first, it is  $G_{S_0} \sqsubset G'$ ,  $e_0 \in G'.E$ , and  $<_{S_0} \dashv\vdash e_0 \sqsubseteq <'$ .

PROOF: From Prop. E.23 and  $\text{next}_P(G_{S_0}) = e_0$ .

⟨3⟩3. LET: Let  $t$  be the last step that revisits  $e_0$  in  $\hat{S}$ , and  $\langle \bar{G}, \bar{<} \rangle$  and  $\langle G'', <'' \rangle$  the configurations that precede and follow  $t$ , respectively.

PROOF: There exists a step that revisits  $e_0$  in  $\hat{S}$  from ⟨3⟩1, ⟨3⟩2, and ⟨1⟩3.

⟨3⟩4.  $G' \supseteq G_c$ , where  $G_p \xrightarrow{w@p} e_0 @w \xrightarrow{} G_c$

PROOF: From ⟨3⟩2 and Lemma E.25.

⟨3⟩5. Q.E.D.

PROOF: From ⟨3⟩4 and ⟨3⟩2,  $w$  must revisit  $e_0$  from an execution  $\bar{G}$ . Then,  $\bar{S}$  is the part of  $\hat{S}$  up to  $\bar{G}$ ,  $\bar{A}$  the events affected by the revisit, and the rest proof obligations follow immediately by the definition of the revisit step and ⟨3⟩2.

⟨2⟩7. LET: Given an iteration with values  $\langle S, A \rangle$ ,

$\langle G(S), <_S \rangle \triangleq \text{APPLY}(S)$  and  $G_{MC}(A) \triangleq \text{MAXCOMPLETION}(G_p, A)$

⟨2⟩8. LET:  $\text{Inv}(S, A)$  be the conjunction of

1.  $G_{MC}(A) \neq \perp$

2.  $S = S_0 \Rightarrow A = \emptyset$

3.  $S \neq S_0 \Rightarrow S_0 \sqsubset S \wedge G_{S_0} \sqsubset G(S) \sqsubseteq G_{MC}(A) \wedge <_{S_0} \dashv\vdash e_0 \sqsubseteq <_S$

4.  $A = \text{sort}_{<_S}(G(S).E \setminus G_p.E)$  and  $w \notin A$

5. If  $\exists e_o \in A$ .  $\text{open}(G(S), e_o)$ , then  $e_o = \text{LAST}(A)$

6. If  $\hat{S} \sqsupset S_0$  and  $\text{APPLY}(\bar{S}) \supseteq G_t$ , then  $\bar{A} \supseteq A$  and  $\bar{S} \supseteq S$  (⟨2⟩6)

⟨2⟩9. At the beginning of an iteration  $\langle S, A \rangle$ :  $\text{Inv}(S, A)$

⟨3⟩1.  $\text{Inv}(S_0, \emptyset)$

PROOF: It is  $G(S_0) = G_{S_0} \sqsubseteq G_p = G_{MC}(\emptyset) \neq \perp$ . The rest follow trivially from  $S = S_0$  and  $A = \emptyset$ .

⟨3⟩2. SUFFICES ASSUME: An iteration  $\langle S, A \rangle$  where  $\text{Inv}(S, A)$  and the test in Line 17 fails

PROVE: It is  $\text{Inv}(S', A')$  for the values  $\langle S', A' \rangle$  at the end of the iteration.

PROOF: ⟨3⟩1 and induction on the number of loop iterations until the test in Line 17 succeeds.

⟨3⟩3.  $G_{S_0} \sqsubseteq G(S) \sqsubseteq G_{MC}(A)$  and  $<_{S_0} \sqsubseteq <_S$

⟨4⟩1.  $G_{S_0} \sqsubseteq G(S_0) \sqsubseteq G_{MC}(\emptyset)$

PROOF: From  $G_{S_0} = G(S_0)$ ,  $G_{MC}(\emptyset) = G_p$ , and  $G_{S_0} \sqsubseteq G_p$  (definition of  $G_p$ ).

⟨4⟩2. Q.E.D.

PROOF: From loop invariants 3, 2, and ⟨4⟩1.

⟨3⟩4.  $e \neq \perp$

⟨4⟩1.  $\text{avail}(G_{MC}(A)) \neq \emptyset$

PROOF: From  $w \in \text{avail}(G_p)$  and  $w \notin A$  (4), we have  $w \in \text{avail}(G_{MC}(A))$ .

⟨4⟩2.  $G(S) \sqsubseteq G_{MC}(A)$

PROOF: From ⟨3⟩3.

⟨4⟩3. Q.E.D.

PROOF: From ⟨4⟩1 and ⟨4⟩2.

⟨3⟩5. CASE:  $e \in G_p.E$

⟨4⟩1.  $A' = A$

⟨4⟩2.  $G_{MC}(A') \neq \perp$

PROOF: From loop invariant 1 and ⟨4⟩1.

⟨4⟩3.  $\text{consistent}_{\text{SYM}}(G_{MC}(A'))$

PROOF: From ⟨2⟩3 and Corollary E.10.



- $\langle 4 \rangle 4.$   $\text{next}_P(G(S)) \in G_{MC}(A')$   
 PROOF: From  $e \in G_p.E \subseteq G_{MC}(A).E = G_{MC}(A').E$  ( $\langle 4 \rangle 1$ ).
- $\langle 4 \rangle 5.$   $G(S) \sqsubset G_{MC}(A')$   
 $\langle 5 \rangle 1.$   $G(S) \sqsubseteq G_{MC}(A')$   
 PROOF: From  $\langle 3 \rangle 3$  and  $\langle 4 \rangle 1$ .  
 $\langle 5 \rangle 2.$   $G(S) \neq G_{MC}(A')$   
 PROOF: From  $\langle 4 \rangle 4$ .  
 $\langle 5 \rangle 3.$  Q.E.D.
- $\langle 4 \rangle 6.$   $\langle -|\text{APPLY}(S).E|, |G_{MC}(A').E| \rangle < M$   
 $\langle 5 \rangle 1.$   $G(S) \supseteq G_{S_0}$   
 PROOF: From  $\langle 3 \rangle 3$ .  
 $\langle 5 \rangle 2.$  CASE:  $G(S) \neq G_{S_0}$   
 PROOF: From  $\langle 5 \rangle 1$  and  $\langle 5 \rangle 2$ , it is  $G(S) \sqsubset G_{S_0}$  and therefore  $-|G(S).E| < -|G_{S_0}.E$ .  
 $\langle 5 \rangle 3.$  CASE:  $G(S) = G_{S_0}$   
 $\langle 6 \rangle 1.$   $\text{next}_P(G(S)) = e_0$   
 PROOF: From  $\langle 5 \rangle 3$  and loop invariant 3 it is  $S = S_0$ .  
 $\langle 6 \rangle 2.$  Q.E.D.  
 PROOF: Contradiction from  $\langle 6 \rangle 1$ ,  $\langle 3 \rangle 5$ , and  $\langle 2 \rangle 5$ .
- $\langle 5 \rangle 4.$  Q.E.D.  
 PROOF: Cases  $\langle 5 \rangle 2$  and  $\langle 5 \rangle 3$  are exhaustive.
- $\langle 4 \rangle 7.$  1.  $S_0 \sqsubset S'$ ,  $\text{APPLY}(S') = \langle G(S'), <_{S'} \rangle$ , and  $G(S) \sqsubset G(S') \sqsubseteq G_{MC}(A')$   
 2.  $<_S \uparrow\uparrow \text{next}_P(G(S)) \sqsubseteq <_{S'}$  and  $\text{LAST}(S')$  either adds or revisits  $\text{next}_P(G(S))$   
 3. If  $\bar{S} \sqsubset S_0$  and  $\text{APPLY}(\bar{S}) \supseteq G_{MC}(A')$ , then  $\bar{S} \supseteq S'$   
 PROOF: From  $\langle 4 \rangle 5$ ,  $\langle 4 \rangle 3$ ,  $\langle 4 \rangle 4$ ,  $\langle 4 \rangle 6$ , and  $\langle 1 \rangle 1$ .
- $\langle 4 \rangle 8.$   $S' \neq S_0$   
 PROOF: From  $\langle 4 \rangle 7:1$ .
- $\langle 4 \rangle 9.$   $S_0 \sqsubset S' \wedge G_{S_0} \sqsubset G(S') \sqsubseteq G_{MC}(A') \wedge <_{S_0} \uparrow\uparrow e_0 \sqsubseteq <'_S$   
 PROOF: From  $\langle 4 \rangle 7$  and  $\langle 3 \rangle 3$ .
- $\langle 4 \rangle 10.$   $A' = \text{sort}_{<_{S'}}(G(S').E \setminus G_p.E)$  and  $w \notin A'$   
 $\langle 5 \rangle 1.$   $A = \text{sort}_{<_S}(G(S).E \setminus G_p.E)$  and  $w \notin A$   
 PROOF: From loop invariant 4.  
 $\langle 5 \rangle 2.$   $G(S').E \setminus G(S).E \subseteq G_p.E$   
 From  $\langle 5 \rangle 1$ , it is  $A' = A \subseteq G(S).E$ , and from  $\langle 4 \rangle 7$  (1) it is  $G(S) \sqsubset G(S') \sqsubseteq G_{MC}(A')$ .  
 $\langle 5 \rangle 3.$   $G(S').E \setminus G_p.E = G(S).E \setminus G_p.E$   
 PROOF: From  $\langle 5 \rangle 2$ .  
 $\langle 5 \rangle 4.$  Q.E.D.  
 PROOF: From  $\langle 5 \rangle 3$ ,  $<_S \sqsubseteq <_{S'}$  ( $\langle 4 \rangle 7:2$ ),  $\langle 5 \rangle 1$ , and  $\langle 4 \rangle 1$ .
- $\langle 4 \rangle 11.$  If  $\exists e_o \in A'. \text{open}(G(S'), e_o)$ , then  $\Rightarrow e_o = \text{LAST}(A')$   
 $\langle 5 \rangle 1.$  If  $\exists e_o \in G(S). \text{open}(G(S'), e_o)$ , then  $\text{open}(G(S), e_o)$   
 PROOF: From  $G(S) \sqsubseteq G(S')$  ( $\langle 4 \rangle 7:1$ ).  
 $\langle 5 \rangle 2.$  Q.E.D.  
 PROOF: From loop invariant 5,  $\langle 5 \rangle 1$ , and  $\langle 4 \rangle 1$ .
- $\langle 4 \rangle 12.$  If  $\hat{S} \sqsubset S_0$  and  $\text{APPLY}(\hat{S}) \supseteq G_t$ , then  $\bar{A} \supseteq A'$  and  $\bar{S} \supseteq S'$   
 $\langle 5 \rangle 1.$  ASSUME:  $\hat{S} \sqsubset S_0$  and  $\text{APPLY}(\hat{S}) \supseteq G_t$   
 $\langle 5 \rangle 2.$   $\bar{A} \supseteq A$  and  $\bar{S} \supseteq S$   
 PROOF: From loop invariant 6 and  $\langle 2 \rangle 6$  (2).  
 $\langle 5 \rangle 3.$   $G_{MC}(A') \sqsubseteq \bar{G}$

- PROOF:  $G_{MC}(A') = G_{MC}(A) \sqsubseteq G_{MC}(\bar{A}) = \bar{G}$  ( $A \sqsubseteq \bar{A}$  from  $\langle 5 \rangle 2$ ).
- $\langle 5 \rangle 4$ .  $\bar{S} \sqsupseteq S'$   
 PROOF: From  $\langle 4 \rangle 7(3)$ ,  $\langle 5 \rangle 1$ , and  $\langle 5 \rangle 3$ .
- $\langle 5 \rangle 5$ . Q.E.D.  
 PROOF: From  $\langle 5 \rangle 2$ ,  $\langle 4 \rangle 1$ , and  $\langle 5 \rangle 4$ .
- $\langle 4 \rangle 13$ . Q.E.D.  
 PROOF: From  $\langle 4 \rangle 2$ ,  $\langle 4 \rangle 8$ ,  $\langle 4 \rangle 9$ ,  $\langle 4 \rangle 10$ ,  $\langle 4 \rangle 11$ , and  $\langle 4 \rangle 12$ .
- $\langle 3 \rangle 6$ . CASE:  $e \notin G_p.E$
- $\langle 4 \rangle 1$ .  $A' = A \uparrow\uparrow e$
- $\langle 4 \rangle 2$ .  $G_{MC}(A') \neq \perp$
- $\langle 5 \rangle 1$ .  $G_{MC}(A) \neq \perp$   
 PROOF: From loop invariant 1.
- $\langle 5 \rangle 2$ .  $dom(G_{MC}(A).symbol; [r]) \subseteq G_{MC}(A).E$   
 PROOF: From  $next_P(G(S)) = e$ , we have  $dom(G(S).symbol; [e]) \subseteq G(S).E$ . The result follows from  $G(S) \sqsubseteq G_{MC}(A)$ .
- $\langle 5 \rangle 3$ . CASE:  $e \in R$   
 PROOF: From definition of  $\rightsquigarrow$  and  $\langle 4 \rangle 1$ .
- $\langle 5 \rangle 4$ . CASE:  $e \in W$
- $\langle 6 \rangle 1$ . There is a matching open read  $e_o$
- $\langle 6 \rangle 2$ .  $e_o \in A$
- $\langle 7 \rangle 1$ .  $e_o \notin G_p$   
 PROOF: From  $\langle 3 \rangle 6$  and  $e_o$  being the matching read of  $e$ .
- $\langle 7 \rangle 2$ .  $G(S) \sqsubseteq G_{MC}(A)$   
 PROOF: From  $\langle 3 \rangle 3$ .
- $\langle 7 \rangle 3$ . Q.E.D.  
 PROOF: From  $\langle 7 \rangle 1$  and  $\langle 7 \rangle 2$ .
- $\langle 6 \rangle 3$ .  $e_o = \text{LAST}(A)$   
 PROOF: From  $\langle 6 \rangle 1$ ,  $\langle 6 \rangle 2$ , and loop invariant 5.
- $\langle 6 \rangle 4$ . Q.E.D.  
 PROOF: From  $\langle 6 \rangle 3$ ,  $\langle 4 \rangle 1$ , and definition of  $\rightsquigarrow$ .
- $\langle 5 \rangle 5$ . Q.E.D.  
 PROOF: From  $\langle 5 \rangle 2$ ,  $\langle 5 \rangle 3$ , and  $\langle 5 \rangle 4$ .
- $\langle 4 \rangle 3$ .  $\text{consistent}_{\text{SYM}}(G_{MC}(A'))$   
 PROOF: From  $\langle 2 \rangle 3$  and Corollary E.10.
- $\langle 4 \rangle 4$ .  $next_P(G) \in G_{MC}(A')$   
 PROOF: From  $\langle 4 \rangle 1$ .
- $\langle 4 \rangle 5$ .  $G(S) \sqsubset G_{MC}(A')$
- $\langle 5 \rangle 1$ .  $G(S) \sqsubseteq G_{MC}(A')$   
 PROOF: From  $\langle 3 \rangle 3$  and  $\langle 4 \rangle 1$ .
- $\langle 5 \rangle 2$ .  $G(S) \neq G_{MC}(A')$   
 PROOF: From  $\langle 4 \rangle 4$ .
- $\langle 5 \rangle 3$ . Q.E.D.
- $\langle 4 \rangle 6$ .  $\langle -|\text{APPLY}(S).E|, |G_{MC}(A').E| \rangle < M$
- $\langle 5 \rangle 1$ .  $G(S) \sqsupseteq G_{S_0}$   
 PROOF: From  $\langle 3 \rangle 3$ .
- $\langle 5 \rangle 2$ . CASE:  $G(S) \neq G_{S_0}$   
 PROOF: From  $\langle 5 \rangle 1$  and  $\langle 5 \rangle 2$ , it is  $G(S) \sqsubset G_{S_0}$  and therefore  $-|G(S).E| < -|G_{S_0}.E|$ .
- $\langle 5 \rangle 3$ . CASE:  $G(S) = G_{S_0}$

- $\langle 6 \rangle 1. S = S_0$   
 PROOF: From loop invariant 3.
- $\langle 6 \rangle 2. A' = [e_0]$   
 PROOF: From loop invariant 2,  $\text{next}_P(G_{S_0}) = e_0$ , and  $\langle 4 \rangle 1$ .
- $\langle 6 \rangle 3. \text{Q.E.D.}$   
 PROOF: It is  $G_{MC}(A').E = G_p.E \cup \{e_0\} \subseteq G_t.E \setminus \{w\}$  and therefore  $|G_{MC}(A').E| < |G_t.E|$ .
- $\langle 5 \rangle 4. \text{Q.E.D.}$   
 PROOF: Cases  $\langle 5 \rangle 2$  and  $\langle 5 \rangle 3$  are exhaustive.
- $\langle 4 \rangle 7. 1. S_0 \sqsubset S', \text{APPLY}(S') = \langle G(S'), <_{S'} \rangle$ , and  $G(S) \sqsubset G(S') \sqsubseteq G_{MC}(A')$   
 2.  $<_S \dashv\vdash \text{next}_P(G(S)) \sqsubseteq <_{S'}$  and  $\text{LAST}(S')$  either adds or revisits  $\text{next}_P(G(S))$   
 3. If  $\bar{S} \sqsupset S_0$  and  $\text{APPLY}(\bar{S}) \sqsupseteq G_{MC}(A')$ , then  $\bar{S} \sqsupseteq S'$   
 PROOF: From  $\langle 4 \rangle 5$ ,  $\langle 4 \rangle 3$ ,  $\langle 4 \rangle 4$ ,  $\langle 4 \rangle 6$ , and  $\langle 1 \rangle 1$ .
- $\langle 4 \rangle 8. S' \neq S_0$   
 PROOF: From  $\langle 4 \rangle 7:1$ .
- $\langle 4 \rangle 9. S_0 \sqsubset S' \wedge G_{S_0} \sqsubset G(S') \sqsubseteq G_{MC}(A') \wedge <_{S_0} \dashv\vdash e_0 \sqsubseteq <_{S'}$   
 PROOF: From  $\langle 4 \rangle 7$  and  $\langle 3 \rangle 3$ .
- $\langle 4 \rangle 10. A' = \text{sort}_{<_{S'}}(G(S').E \setminus G_p.E)$  and  $w \notin A'$   
 $\langle 5 \rangle 1. A = \text{sort}_{<_S}(G(S).E \setminus G_p.E)$  and  $w \notin A$   
 PROOF: From loop invariant 4.
- $\langle 5 \rangle 2. w \notin A'$   
 PROOF: From  $\langle 5 \rangle 1$  and  $e \neq w$  ( $\langle 3 \rangle 2$ ).
- $\langle 5 \rangle 3. G(S').E \setminus G(S).E \subseteq G_p.E \cup \{e\}$   
 From  $A \subseteq G(S).E$  ( $\langle 5 \rangle 1$ ),  $\langle 4 \rangle 9$ , and  $\langle 4 \rangle 1$ .
- $\langle 5 \rangle 4. G(S').E \setminus G_p.E = (G(S).E \setminus G_p.E) \cup \{e\}$   
 PROOF: From  $\langle 5 \rangle 3$ .
- $\langle 5 \rangle 5. \text{Q.E.D.}$   
 PROOF: From  $\langle 5 \rangle 4$ ,  $<_S \sqsubseteq <_{S'}$  ( $\langle 4 \rangle 7:2$ ),  $\langle 5 \rangle 1$ , and  $\langle 4 \rangle 1$ .
- $\langle 4 \rangle 11. \text{If } \exists e_o \in A'. \text{open}(G(S'), e_o), \text{ then } \Rightarrow e_o = \text{LAST}(A')$   
 PROOF: From  $\langle 4 \rangle 7$   $\text{LAST}(S')$  either adds or revisits  $e$  and from Prop. E.22, if there is an open read in  $G'$ , it is just added or revisited. Therefore, if there is an open read, it is  $e = \text{LAST}(A')$ .
- $\langle 4 \rangle 12. \text{If } \hat{S} \sqsupset S_0 \text{ and } \text{APPLY}(\hat{S}) \sqsupseteq G_t, \text{ then } \bar{A} \sqsupseteq A' \text{ and } \bar{S} \sqsupseteq S'$   
 $\langle 5 \rangle 1. \text{ASSUME: } \hat{S} \sqsupset S_0 \text{ and } \text{APPLY}(\hat{S}) \sqsupseteq G_t$   
 $\langle 5 \rangle 2. \bar{A} \sqsupseteq A \text{ and } \bar{S} \sqsupseteq S$   
 PROOF: From loop invariant 6 and  $\langle 2 \rangle 6$  (2).
- $\langle 5 \rangle 3. G_{MC}(A) \sqsubseteq \bar{G}$   
 PROOF:  $G_{MC}(A) \sqsubseteq G_{MC}(\bar{A}) = \bar{G}$  ( $A \sqsubseteq \bar{A}$  from  $\langle 5 \rangle 2$ ).
- $\langle 5 \rangle 4. \bar{S} \sqsupset S$   
 PROOF: From  $\langle 5 \rangle 2$  and  $\text{next}_P(G) = e \neq w = \text{next}_P(\bar{G})$  ( $\langle 3 \rangle 2$ ).
- $\langle 5 \rangle 5. e \in \bar{G}.E$  and  $<_S \dashv\vdash e \sqsubseteq \bar{\phantom{x}}$   
 PROOF: From  $\langle 5 \rangle 3$ ,  $\langle 5 \rangle 4$ , and Prop. E.23.
- $\langle 5 \rangle 6. \bar{A} \sqsupseteq A'$   
 PROOF: From  $\langle 5 \rangle 2$ ,  $\langle 5 \rangle 5$ ,  $\langle 3 \rangle 6$ , and definition of  $\bar{A}$  ( $\langle 2 \rangle 6:5$ ).
- $\langle 5 \rangle 7. G_{MC}(A') \sqsubseteq \bar{G}$   
 PROOF: From  $\langle 5 \rangle 6$ .
- $\langle 5 \rangle 8. \bar{S} \sqsupseteq S'$

PROOF: From  $\langle 4 \rangle 7$  (3),  $\langle 5 \rangle 4$ , and  $\langle 5 \rangle 8$ .

$\langle 5 \rangle 9$ . Q.E.D.

PROOF: From  $\langle 5 \rangle 6$  and  $\langle 5 \rangle 8$ .

$\langle 4 \rangle 13$ . Q.E.D.

PROOF: From  $\langle 4 \rangle 2$ ,  $\langle 4 \rangle 8$ ,  $\langle 4 \rangle 9$ ,  $\langle 4 \rangle 10$ ,  $\langle 4 \rangle 11$ , and  $\langle 4 \rangle 12$ .

$\langle 2 \rangle 10$ . LET: 1.  $\langle S_l, A_l \rangle$  be the values at the last iteration.

2.  $\langle G_l, <_l \rangle \triangleq \text{APPLY}(S_l)$

3.  $P \triangleq \text{dom}((G_l \uplus \{w\}).\text{porf}; [\{w\}])$

4.  $S'$  be the return value in Line 18

PROOF: The loop will eventually terminate because at each iteration, the size of the execution increases ( $G(S) \sqsubset G(S')$ ), and the program semantics only contain executions of finite size.

$\langle 2 \rangle 11$ .  $\text{Inv}(S_l, A_l)$

PROOF: From  $\langle 2 \rangle 9$ .

$\langle 2 \rangle 12$ .  $\text{next}_P(G_l) = w$

PROOF: The test in Line 17 succeeds.

$\langle 2 \rangle 13$ .  $S_0 \neq S_l$

PROOF:  $\text{next}_P(G_{S_0}) = e_0 \neq w = \text{next}_P(G_l)$  ( $\langle 2 \rangle 13$ ).

$\langle 2 \rangle 14$ .  $G_l = \text{MAXCOMPLETION}(G_p, A_l)$

PROOF: From  $\langle 2 \rangle 13$ ,  $\langle 2 \rangle 11:3$ ,  $\langle 2 \rangle 12$ , and definition of  $w$  ( $\langle 2 \rangle 2$ ): all event in  $G_p$  must have already been added.

$\langle 2 \rangle 15$ .  $\{e' \in G_l.E \mid e' <_l e_0\} = G_{S_0}.E$

PROOF: From  $G_{S_0} \sqsubseteq G_l$  ( $\langle 2 \rangle 14$ ),  $\langle 2 \rangle 13$ , and Prop. E.23.

$\langle 2 \rangle 16$ .  $A_l = \text{sort}_{<}(\{e' \in G_l.E \setminus P \mid e_0 \leq e'\})_{<}$

PROOF: From  $\langle 2 \rangle 15$  and  $\langle 2 \rangle 11:4$ .

$\langle 2 \rangle 17$ . LET:  $G' : G_p \xrightarrow{w@P} e_0@w \rightarrow G'$

$\langle 2 \rangle 18$ .  $\text{consistent}_{\text{SYM}}(G')$

PROOF: From Corollary E.11 ( $G' \sqsubseteq G_t$ ).

$\langle 2 \rangle 19$ . LET:  $S'$  be the production sequence in Line 18

$\langle 2 \rangle 20$ .  $\text{APPLY}(S') = \langle G', <' \rangle$

PROOF: The revisit step is enabled:  $\langle 2 \rangle 12$ ,  $\langle 2 \rangle 14$ ,  $\langle 2 \rangle 16$ , and  $\langle 2 \rangle 18$ .

$\langle 2 \rangle 21$ .  $S_0 \sqsubset S'$

PROOF:  $S_0 \sqsubseteq S_l$  ( $\langle 2 \rangle 13$  and  $\langle 2 \rangle 11:3$ ) and  $S_l \sqsubset S'$ .

$\langle 2 \rangle 22$ .  $\text{LAST}(S')$  revisits  $e_0$

$\langle 2 \rangle 23$ .  $<_{S_0} \uparrow\uparrow e_0 \sqsubseteq <'$

PROOF: From  $\langle 2 \rangle 11:3$  and  $\langle 2 \rangle 21$ .

$\langle 2 \rangle 24$ . If  $\hat{S} \sqsupset S_0$  and  $\text{APPLY}(\hat{S}) \sqsupseteq G_t$ , then  $\hat{S} \sqsupseteq S'$

$\langle 3 \rangle 1$ .  $\bar{S} = S_l$

PROOF: It is  $S_l \sqsubseteq \bar{S}$  and  $G_l \sqsubseteq \bar{G}$  ( $\langle 2 \rangle 11:6$ ), and if  $S_l \sqsubset \bar{S}$ , we have  $w \in \bar{G}$  from Prop. E.23, which contradicts  $\text{next}_P(\bar{G}) = w$ .

$\langle 3 \rangle 2$ . Q.E.D.

PROOF: From  $\langle 3 \rangle 1$  and  $S_l \sqsubseteq S'$ .

$\langle 2 \rangle 25$ . Q.E.D.

PROOF: From  $\langle 2 \rangle 20$ ,  $\langle 2 \rangle 21$ ,  $\langle 2 \rangle 22$ ,  $\langle 2 \rangle 23$ , and  $\langle 2 \rangle 24$ .

$\langle 1 \rangle 4$ . Q.E.D.

PROOF: From  $\langle 1 \rangle 1$  and the fact that cases  $\langle 1 \rangle 2$  and  $\langle 1 \rangle 3$  are exhaustive.  $\square$

**THEOREM E.27.** *Given an execution  $G_f \in \llbracket P \rrbracket_M^{\text{Annot}}$  such that  $\text{ACYCLIC}(G_f.\text{cb}_{\text{SYM}})$ ,  $\text{PRODUCTIONSEQUENCE}(G_f)$  will return the unique production sequence  $S$  such that  $\text{APPLY}(S) = G_f$ .*

PROOF. We will show that  $\text{PRODUCTIONSEQUENCE}(G_f)$  returns a production sequence  $S_f$  such that  $\text{APPLY}(S_f) = G_f$ , and if there is a production sequence  $\hat{S}$  such that  $\text{APPLY}(\hat{S}) = G_f$ , it is  $\hat{S} = S_f$ . We will prove that at the beginning of every iteration of  $\text{PRODUCTIONSEQUENCE}(G_f)$  where  $G \triangleq \text{APPLY}(S)$ , it is  $S \sqsubseteq \hat{S}$  and either  $G = G_f$  or  $G \sqsubset G_f$  and  $G \sqsubset G'$  where  $G' = \text{APPLY}(S')$  and  $S'$  is the value of  $S$  at the end of the iteration.

Since  $G_f$  is full,  $\text{dom}(G_f.\text{symb}; [G_f.E]) \subseteq G_f.E$ . From the hypothesis, it is also  $\text{ACYCLIC}(G_f.\text{cb}_{\text{SYM}})$ , and therefore, from Prop. E.12,  $G_\emptyset \sqsubseteq G_f$ . Therefore, from the first iteration it is  $\emptyset \sqsubseteq \hat{S}$  and either  $G_f = G_\emptyset$  or  $G_\emptyset \sqsubset G_f$ . For any other iteration before the loop terminates with  $G \sqsubset G_f$  and  $S \sqsubseteq \hat{S}$ , we have  $\text{next}_P(G) \in G_f.E$  because  $G_f$  is full, and  $\text{consistent}_{\text{SYM}}(G_f)$  from the hypothesis, and therefore  $G \sqsubset G' \sqsubseteq G_t$  and  $S' \sqsubseteq \hat{S}$  from Lemma E.26.

The loop will terminate since the program semantics only contain executions of finite size and  $\text{consistent}_{\text{SYM}}(G)$ . For the final value  $S_f$ , it is  $\text{APPLY}(S_f) = G_f$ , and  $S_f \sqsubseteq \hat{S}$ . Since  $G_f$  is full, there is no other step to be taken from  $S_f$ , and therefore  $\hat{S} = S_f$ .  $\square$

## F External Symmetries

LEMMA F.1. *Let  $G$  be an execution s.t.  $\text{consistent}_{\text{SYM}}(G)$  with a  $\text{cb}_{\text{SYM}}$  cycle. Then  $G$  has a  $\text{po} \cup \text{rf} \cup \text{co}$  cycle.*

PROOF. Assume the opposite. Let  $C$  be the set of  $G.\text{po} \cup G.\text{rf} \cup G.\text{co} \cup G.\text{symp}$  cycles. Since there is a  $G.\text{cb}_{\text{SYM}}$  cycle,  $C$  is non-empty. Let  $c$  be a cycle of  $C$  with the minimal number of  $G.\text{symp}$  edges. Since  $G.\text{po} \cup G.\text{rf} \cup G.\text{co}$  is acyclic,  $c$  has at least one  $G.\text{symp}$  edge  $e = \langle x, y \rangle$ . It must be that  $e$  is between read events, otherwise it can be rewritten as  $G.\text{co}$  ( $G.\text{symp} \cap G.\text{co}^{-1} = \emptyset$ ), contradicting that  $c$  has the minimal number  $G.\text{symp}$  edges among the cycles of  $C$ . Edge  $e$  cannot be the only edge of  $c$  since  $G.\text{symp}$  is irreflexive. Let  $p$  be the path of  $c$  excluding the edge  $e$ . If  $p$  ends with a  $G.\text{po}$  edge, then there is also a cycle that uses  $p$  to enter the thread of  $y$  instead of  $x$ , i.e., it has one less  $G.\text{symp}$  edge, and thus again contradicts the hypothesis about  $c$ . For the same reason  $p$  cannot end with a  $G.\text{symp}$  edge:  $G.\text{symp}$  is transitive and the cycle could be written by combining two consecutive  $G.\text{symp}$  edges. Therefore,  $p$  ends with a  $G.\text{rf}$  edge. It must be that  $x$  and  $y$  read from different writes, otherwise  $c$  can be rewritten by using the  $G.\text{rf}$  edge that ends in  $y$ , avoiding again edge  $e$ . Since  $x$  and  $y$  read from different writes,  $\langle x, y \rangle \in G.\text{symp}$ , and  $G.\text{symp} \cap G.\text{eco}^{-1} = \emptyset$ , it is  $\langle x, y \rangle \in G.\text{eco}$ , and thus  $\langle x, y \rangle \in G.\text{rb}; G.\text{rf}$ . Therefore the cycle  $c$  is  $p'; G.\text{rf}; [x]; G.\text{rf}^{-1}; G.\text{co}; G.\text{rf}; [y]$  which can be rewritten as  $p'; G.\text{co}; G.\text{rf}$ . This again contradicts the assumption that  $c$  is the cycle of  $C$  with the minimal number of  $G.\text{symp}$  edges, concluding the proof.  $\square$

PROPOSITION F.2 (**cb<sub>SYM</sub> CYCLE**). *If there is an execution  $G \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  with a  $G.\text{cb}_{\text{SYM}}$  cycle, then there is an execution  $G' \in \llbracket P \rrbracket_{\text{SYM}}^{\text{Annot}}$  such that  $\text{IRREFLEXIVE}(G'.\text{cb}_{\text{SYM}})$  and  $G'$  has a  $\text{po} \cup \text{rf} \cup \text{co}$  cycle.*

PROOF. From Lemma F.1,  $G$  has a  $\text{po} \cup \text{rf} \cup \text{co}$  cycle. Let  $G'$  be a maximal  $\text{porf}$ -prefix of  $G$  s.t.  $G'$  has no  $\text{po} \cup \text{rf} \cup \text{co}$  cycle, i.e., extending by any other event of  $G$  introduces such a cycle. Let  $e$  be any such event and  $G''$  the resulting execution. Observe that  $e$  must be a write: adding any read event cannot introduce such a cycle. From Lemma F.1,  $G'$  has no  $\text{cb}_{\text{SYM}}$  cycle. Since  $G'$  and  $G''$  only differ by the write  $e$ ,  $G''$  also has no  $\text{cb}_{\text{SYM}}$  cycle: any such cycle must include a  $\text{po}$  edge from an event  $x$  to  $e$  followed by a  $\text{symp}$  edge to  $y$ , which can also be rewritten to avoid  $e$  (there exists an  $\text{symp}; \text{po}$  edge from  $x$  to  $y$ ). We can now sort any symmetric threads that are incomparable w.r.t. to  $\text{eco}$  (lexicographically, in  $\text{po}$  order, i.e., one is a prefix of the other) in decreasing thread length. This reordering cannot introduce any  $\text{cb}_{\text{SYM}}$ -cycles (no  $\text{symp}$  edge is added), and, by construction, for the resulting execution,  $\text{symp}$  is backward-closed and respects  $\text{eco}$ . Therefore, we can maximally extend it in left-to-right thread order, and obtain a consistent,  $\text{cb}_{\text{SYM}}$ -acyclic execution whose  $\text{symp}$  respects  $\text{eco}$  and has a  $\text{po} \cup \text{rf} \cup \text{co}$  cycle.  $\square$

## G Experiments

In what follows, “Execs” denotes the number of complete executions explored, and “Blocked” denotes the number of blocked executions explored (e.g., due to an assume failing). We do not report times as all tools are based on the same implementation, and time is directly proportionate to the execution number. For the comparison with NIDHUGG, we only use non-data-structure benchmarks because NIDHUGG does not support hazard pointers, as a result of which it cannot handle our queue benchmarks.

Table 1. Multiset client

	SR		TruSt		DPOR+IS		DPOR+SR		SPORE	
	Execs	Blocked	Execs	Blocked	Execs	Blocked	Execs	Blocked	Execs	Blocked
msqueue(1)	1	0	1	0	1	0	1	0	1	0
msqueue(2)	37	0	3	1	2	1	3	1	2	0
msqueue(3)	⊖	⊖	26	38	6	14	13	19	3	0
msqueue(4)	⊖	⊖	158	694	22	102	41	179	6	4
msqueue(5)	⊖	⊖	4638	30 402	114	1230	397	2623	10	9
msqueue(6)	⊖	⊖	43 434	783 193	618	16 740	1284	23 368	20	69
msqueue(7)	⊖	⊖	⊖	⊖	4560	278 432	22 469	564 441	35	155
msqueue(8)	⊖	⊖	⊖	⊖	32 760	5 490 520	⊖	⊖	70	965
dglmqueue(1)	1	0	1	0	1	0	1	0	1	0
dglmqueue(2)	10	0	4	0	3	0	4	0	3	0
dglmqueue(3)	32 313	0	34	32	8	12	17	16	4	0
dglmqueue(4)	⊖	⊖	286	416	50	92	73	106	13	3
dglmqueue(5)	⊖	⊖	10 926	20 964	246	1188	921	1790	21	4
dglmqueue(6)	⊖	⊖	145 926	411 695	2454	14 316	4206	12 151	73	36
dglmqueue(7)	⊖	⊖	⊖	⊖	18 744	229 672	118 857	336 550	136	55
dglmqueue(8)	⊖	⊖	⊖	⊖	263 064	3 829 296	573 105	2 508 330	501	390
folqueue(1)	1	0	1	0	1	0	1	0	1	0
folqueue(2)	357	0	4	2	3	1	4	2	3	1
folqueue(3)	⊖	⊖	48	24	12	6	48	24	12	6
folqueue(4)	⊖	⊖	358	1418	58	204	182	718	30	81
folqueue(5)	⊖	⊖	15 318	72 069	414	2002	7722	36 249	210	822
folqueue(6)	⊖	⊖	170 514	3 474 177	2796	65 521	29 406	611 749	504	8488
folqueue(7)	⊖	⊖	⊖	⊖	28 968	931 053	⊖	⊖	5040	127 172
folqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	11 880	1 367 168
treiber(1)	1	0	1	0	1	0	1	0	1	0
treiber(2)	2	0	2	0	2	0	2	0	2	0
treiber(3)	183	0	8	6	8	6	4	3	4	3
treiber(4)	13 190	0	38	32	38	32	10	9	10	9
treiber(5)	⊖	⊖	282	645	282	645	24	59	24	59
treiber(6)	⊖	⊖	2292	5736	2292	5736	68	191	68	191
treiber(7)	⊖	⊖	24 576	131 752	24 576	131 752	176	1066	176	1066
treiber(8)	⊖	⊖	292 920	1 683 556	292 920	1 683 556	546	3682	546	3682

Table 2. LIFO/FIFO client

	SR		TruSt		DPOR+IS		DPOR+SR		SPORE	
	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>
msqueue(1)	⊖	⊖	181	316	15	54	181	316	15	16
msqueue(2)	⊖	⊖	1714	12 425	72	790	1714	12 425	72	313
msqueue(3)	⊖	⊖	121 832	1 093 531	672	12 772	60 916	548 202	336	2030
msqueue(4)	⊖	⊖	⊖	⊖	4344	272 652	⊖	⊖	930	14 463
msqueue(5)	⊖	⊖	⊖	⊖	49 560	5 787 820	⊖	⊖	3580	70 700
msqueue(6)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	8240	430 480
msqueue(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	28 740	1 835 111
msqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
<hr/>										
dglmqueue(1)	⊖	⊖	315	399	27	63	315	399	27	28
dglmqueue(2)	⊖	⊖	4275	9592	252	892	4275	9592	252	435
dglmqueue(3)	⊖	⊖	414 904	1 057 713	2040	14 944	207 452	529 850	1020	2674
dglmqueue(4)	⊖	⊖	⊖	⊖	27 108	270 608	1 993 212	8 081 770	6606	19 707
dglmqueue(5)	⊖	⊖	⊖	⊖	304 680	5 507 860	⊖	⊖	24 760	85 831
dglmqueue(6)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	134 060	519 354
dglmqueue(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	498 525	2 008 304
dglmqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
<hr/>										
folqueue(1)	⊖	⊖	642	251	69	32	642	251	69	32
folqueue(2)	⊖	⊖	6993	42 493	390	2619	6993	42 493	390	2124
folqueue(3)	⊖	⊖	754 830	4 717 584	5004	35 037	754 830	4 717 584	5004	29 122
folqueue(4)	⊖	⊖	⊖	⊖	38 352	1 797 068	⊖	⊖	18 288	536 895
folqueue(5)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(6)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
<hr/>										
treiber(1)	40 934	0	7	8	7	8	7	8	7	8
treiber(2)	⊖	⊖	56	95	56	95	56	95	56	95
treiber(3)	⊖	⊖	642	1793	642	1793	321	914	321	914
treiber(4)	⊖	⊖	7172	27 939	7172	27 939	1808	7255	1808	7255
treiber(5)	⊖	⊖	109 296	666 885	109 296	666 885	9148	58 610	9148	58 610
treiber(6)	⊖	⊖	⊖	⊖	⊖	⊖	45 590	387 936	45 590	387 936
treiber(7)	⊖	⊖	⊖	⊖	⊖	⊖	211 235	2 886 319	211 235	2 886 319
treiber(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖



Table 3. Emptiness client

	SR		TruST		DPOR+IS		DPOR+SR		SPoRE	
	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>	<i>Execs</i>	<i>Blocked</i>
msqueue(1)	1	0	1	0	1	0	1	0	1	0
msqueue(2)	13 554	0	16	48	6	16	8	24	3	6
msqueue(3)	⊖	⊖	1368	15 350	90	1003	228	2574	15	90
msqueue(4)	⊖	⊖	⊖	⊖	2520	108 696	16 188	634 944	105	1967
msqueue(5)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	945	57 559
msqueue(6)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	10 395	2 195 070
msqueue(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
msqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
dglmqueue(1)	1	0	1	0	1	0	1	0	1	0
dglmqueue(2)	17 146	0	16	40	6	13	8	20	3	4
dglmqueue(3)	⊖	⊖	1488	9990	102	611	248	1661	17	52
dglmqueue(4)	⊖	⊖	⊖	⊖	3672	47 640	20 680	311 868	153	904
dglmqueue(5)	⊖	⊖	⊖	⊖	238 680	6 154 014	⊖	⊖	1989	20 587
dglmqueue(6)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	35 115	601 822
dglmqueue(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
dglmqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(1)	1	0	1	0	1	0	1	0	1	0
folqueue(2)	⊖	⊖	20	54	8	18	20	54	8	18
folqueue(3)	⊖	⊖	2160	24 849	168	1786	2160	24 849	168	1465
folqueue(4)	⊖	⊖	⊖	⊖	6720	340 861	⊖	⊖	6720	236 771
folqueue(5)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(6)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
folqueue(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
treiber(1)	1	0	1	0	1	0	1	0	1	0
treiber(2)	927	0	10	6	10	6	5	3	5	3
treiber(3)	⊖	⊖	270	387	270	387	45	65	45	65
treiber(4)	⊖	⊖	13 992	38 536	13 992	38 536	583	1615	583	1615
treiber(5)	⊖	⊖	1 188 600	5 740 545	1 188 600	5 740 545	9905	48 052	9905	48 052
treiber(6)	⊖	⊖	⊖	⊖	⊖	⊖	209 141	1 694 732	209 141	1 694 732
treiber(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
treiber(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖

Table 4. Non-data-structure benchmarks

	SR		TruSt		DPOR+IS		DPOR+SR		SPORE	
	Execs	Blocked	Execs	Blocked	Execs	Blocked	Execs	Blocked	Execs	Blocked
ttaslock(1)	1	0	1	0	1	0	1	0	1	0
ttaslock(2)	⊖	⊖	4	0	4	0	2	0	2	0
ttaslock(3)	⊖	⊖	36	0	36	0	6	0	6	0
ttaslock(4)	⊖	⊖	576	0	576	0	24	0	24	0
ttaslock(5)	⊖	⊖	14 400	0	14 400	0	120	0	120	0
ttaslock(6)	⊖	⊖	518 400	0	518 400	0	720	0	720	0
ttaslock(7)	⊖	⊖	⊖	⊖	⊖	⊖	5040	0	5040	0
ttaslock(8)	⊖	⊖	⊖	⊖	⊖	⊖	40 320	0	40 320	0
twalock(1)	1	0	1	0	1	0	1	0	1	0
twalock(2)	⊖	⊖	4	0	4	0	2	0	2	0
twalock(3)	⊖	⊖	96	0	96	0	16	0	16	0
twalock(4)	⊖	⊖	6144	0	6144	0	256	0	256	0
twalock(5)	⊖	⊖	798 720	0	798 720	0	6656	0	6656	0
twalock(6)	⊖	⊖	⊖	⊖	⊖	⊖	252 928	0	252 928	0
twalock(7)	⊖	⊖	⊖	⊖	⊖	⊖	13 152 256	0	13 152 256	0
twalock(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
rdcss(1)	98 681	0	51	56	7	6	26	27	4	3
rdcss(2)	⊖	⊖	2296	4048	48	60	580	958	14	16
rdcss(3)	⊖	⊖	250 219	632 803	503	822	20 988	49 953	51	83
rdcss(4)	⊖	⊖	⊖	⊖	7302	14 686	1 139 613	3 677 091	194	428
rdcss(5)	⊖	⊖	⊖	⊖	138 787	330 889	⊖	⊖	772	2234
rdcss(6)	⊖	⊖	⊖	⊖	3 315 560	9 122 025	⊖	⊖	3212	11 874
rdcss(7)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	13 952	64 459
rdcss(8)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	63 150	357 813

Table 5. NIDHUGG, TruSt and SPORE on non-data-structure benchmarks

	NIDHUGG			TruSt			SPORE		
	Execs	Blocked	Time	Execs	Blocked	Time	Execs	Blocked	Time
ttaslock(3,1)	36	39	0.14	36	0	0.12	6	0	0.09
ttaslock(4,1)	576	1084	0.44	576	0	0.14	24	0	0.09
ttaslock(5,1)	14 400	42 845	12.97	14 400	0	1.41	120	0	0.12
ttaslock(6,1)	518 400	2 320 386	759.18	518 400	0	56.14	720	0	0.17
ttaslock(7,1)	⊖	⊖	⊖	⊖	⊖	⊖	5040	0	0.63
ttaslock(8,1)	⊖	⊖	⊖	⊖	⊖	⊖	40 320	0	5.21
ttaslock(3,2)	7134	11 223	4.12	7134	0	0.73	1189	0	0.21
ttaslock(4,2)	⊖	⊖	⊖	5 189 880	0	568.32	216 245	0	24.09
ttaslock(5,2)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
ttaslock(6,2)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
twalock(3,1)	96	0	0.14	96	0	0.35	16	0	0.34
twalock(4,1)	6144	0	1.71	6144	0	0.92	256	0	0.35
twalock(5,1)	798 720	0	263.18	798 720	0	95.88	6656	0	0.77
twalock(6,1)	⊖	⊖	⊖	⊖	⊖	⊖	252 928	0	16.68
twalock(7,1)	⊖	⊖	⊖	⊖	⊖	⊖	13 152 256	0	936.36
twalock(3,2)	84 936	0	25.58	84 936	0	10.12	14 156	0	1.75
twalock(4,2)	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖	⊖
rdcss(1,2)	51	59	0.19	51	56	0.12	4	3	0.11
rdcss(2,2)	2296	4754	2.80	2296	4048	0.62	14	16	0.11
rdcss(3,2)	250 219	821 903	536.00	250 219	632 803	62.57	51	83	0.13
rdcss(4,2)	⊖	⊖	⊖	⊖	⊖	⊖	194	428	0.21
rdcss(5,2)	⊖	⊖	⊖	⊖	⊖	⊖	772	2234	0.64
rdcss(6,2)	⊖	⊖	⊖	⊖	⊖	⊖	3212	11 874	3.00
rdcss(7,2)	⊖	⊖	⊖	⊖	⊖	⊖	13 952	64 459	16.58
rdcss(8,2)	⊖	⊖	⊖	⊖	⊖	⊖	63 150	357 813	94.05

## H Client code

### H.1 Multiset client

```

#include <stdio.h>
#include <stdlib.h>
#include <pthread.h>
#include <stdbool.h>
#include <stdatomic.h>
#include <assert.h>

#include "../lib/queue-wrapper.h"

#ifndef MAX_THREADS
# define MAX_THREADS 32
#endif

#ifdef READERS
#define DEFAULT_READERS (READERS)
#else
#define DEFAULT_READERS 1
#endif

#ifdef WRITERS
#define DEFAULT_WRITERS (WRITERS)
#else
#define DEFAULT_WRITERS 1
#endif

#ifndef HP_THREAD_LIMIT
# define HP_THREAD_LIMIT 32
#endif

int readers = DEFAULT_READERS, writers = DEFAULT_WRITERS;

queue_t *queue;
queue_t myqueue;
int num_threads;

unsigned int input[MAX_THREADS + 1];
unsigned int output[MAX_THREADS + 1];

int __thread tid;

__VERIFIER_hp_t hps[MAX_THREADS + 1][HP_THREAD_LIMIT];
int __thread __hp_index;

/* Keep track of how many readers failed */
bool failed[DEFAULT_READERS];

void set_thread_num(int i)
{
    tid = i;
}

int get_thread_num()
{
    return tid;
}

__VERIFIER_hp_t *get_free_hp()
{
    int index = __hp_index++;
    assert(index < HP_THREAD_LIMIT);
    return &hps[tid][index];
}

void *threadW(void *param)
{
    int pid = (intptr_t) param;

```

```

    set_thread_num(pid);

    input[pid] = pid + 42;
    enqueue(queue, input[pid]);
    return NULL;
}

void *threadR(void *param)
{
    int pid = (intptr_t) param;

    set_thread_num(pid);

    /* UB if we mod with READERS == 0, but that's OK because
     * then this function will not be executed */
    failed[pid % DEFAULT_READERS] = !dequeue(queue, &output[pid]);
    return NULL;
}

int main()
{
    pthread_t threads[MAX_THREADS + 1];
    unsigned int in_sum = 0, out_sum = 0;
    int i = 0;

    queue = &myqueue;
    num_threads = readers + writers;

    init_queue(queue, num_threads);

    ++i;
    for (int j = 0; j < writers; j++, i++) {
        if (j == 0)
            pthread_create(&threads[i], NULL, threadW, (void *) (intptr_t) i);
        else
            threads[i] = __VERIFIER_spawn_symmetric(threadW, (void *) (intptr_t) i, threads[i-1]);
    }
    for (int j = 0; j < readers; j++, i++) {
        if (j == 0)
            pthread_create(&threads[i], NULL, threadR, (void *) (intptr_t) i);
        else
            threads[i] = __VERIFIER_spawn_symmetric(threadR, (void *) (intptr_t) i, threads[i-1]);
    }

    i = 1;
    for (int j = 0; j < writers; j++, i++) {
        if (j == 0)
            pthread_join(threads[i], NULL);
        else
            __VERIFIER_join_symmetric(threads[i]);
    }
    for (int j = 0; j < readers; j++, i++) {
        if (j == 0)
            pthread_join(threads[i], NULL);
        else
            __VERIFIER_join_symmetric(threads[i]);
    }

#ifdef PRINT_INFO
    printf("---\n");
    for (i = 1; i <= num_threads; i++)
        printf("input[%d] = %u, output[%d] = %u\n", i, input[i], i, output[i]);
#endif

    /* Dequeue whatever is left in the queue */
    unsigned tmp;
    while (dequeue(queue, &tmp))
        out_sum += tmp;

    /* Ensure that in_sum == out_sum */
    for (i = 1; i <= num_threads; i++) {

```

```

    in_sum += input[i];
    out_sum += output[i];
}
assert(in_sum == out_sum);

return 0;
}

```

## H.2 FIFO client

```

#include <stdio.h>
#include <stdlib.h>
#include <pthread.h>
#include <stdbool.h>
#include <stdatomic.h>
#include <assert.h>

#include "../lib/queue-wrapper.h"

#ifndef MAX_THREADS
#define MAX_THREADS 32
#endif

#ifndef HP_THREAD_LIMIT
#define HP_THREAD_LIMIT 32
#endif

#ifdef NOISE_ENQ
#define DEFAULT_NOISE_ENQ (NOISE_ENQ)
#else
#define DEFAULT_NOISE_ENQ 1
#endif

#ifdef NOISE_DEQ
#define DEFAULT_NOISE_DEQ (NOISE_DEQ)
#else
#define DEFAULT_NOISE_DEQ 0
#endif

queue_t *queue;
queue_t myqueue;
int num_threads;

int __thread tid;

__VERIFIER_hp_t hps[MAX_THREADS + 1][HP_THREAD_LIMIT];
int __thread __hp_index;

void set_thread_num(int i)
{
    tid = i;
}

int get_thread_num()
{
    return tid;
}

__VERIFIER_hp_t *get_free_hp()
{
    int index = __hp_index++;
    assert(index < HP_THREAD_LIMIT);
    return &hps[tid][index];
}

void *thread_enq(void *param)
{
    int pid = (intptr_t) param;

```

```

    set_thread_num(pid);
    enqueue(queue, 1);
    enqueue(queue, 2);
    return NULL;
}

void *thread_deq(void *param)
{
    int pid = (intptr_t) param;
    unsigned dequeued[2];

    set_thread_num(pid);

    /* Ensure FIFO */
    __VERIFIER_assume(dequeue(queue, &dequeued[0]));
    __VERIFIER_assume(dequeue(queue, &dequeued[1]));
    assert(!(dequeued[0] == 2 && dequeued[1] == 1));
    return NULL;
}

void *noise_enq(void *param)
{
    int pid = (intptr_t) param;

    set_thread_num(pid);
    enqueue(queue, 0);
    return NULL;
}

void *noise_deq(void *param)
{
    int pid = (intptr_t) param;
    unsigned val;

    set_thread_num(pid);
    dequeue(queue, &val);
    return NULL;
}

int main()
{
    pthread_t te, td, noise[DEFAULT_NOISE_ENQ + DEFAULT_NOISE_DEQ + 2];

    queue = &myqueue;
    num_threads = 2 + DEFAULT_NOISE_ENQ + DEFAULT_NOISE_DEQ;

    init_queue(queue, num_threads);

    pthread_create(&te, NULL, thread_enq, (void *) (intptr_t) 1);
    pthread_create(&td, NULL, thread_deq, (void *) (intptr_t) 2);
    int i = 1;
    for (int j = 1; j <= DEFAULT_NOISE_ENQ; j++, i++) {
        if (j == 1)
            pthread_create(&noise[i], NULL, noise_enq, (void *) (intptr_t) 2 + i);
        else
            noise[i] = __VERIFIER_spawn_symmetric(noise_enq, (void *) (intptr_t) 2
+ i, noise[i-1]);
    }
    for (int j = 1; j <= DEFAULT_NOISE_DEQ; j++, i++) {
        if (j == 1)
            pthread_create(&noise[i], NULL, noise_deq, (void *) (intptr_t) 2 + i);
        else
            noise[i] = __VERIFIER_spawn_symmetric(noise_deq, (void *) (intptr_t) 2
+ i, noise[i-1]);
    }

    pthread_join(te, NULL);
    pthread_join(td, NULL);
    i = 1;
    for (int j = 1; j <= DEFAULT_NOISE_ENQ; j++, i++) {
        if (j == 1)

```

```

        pthread_join(noise[i], NULL);
    else
        __VERIFIER_join_symmetric(noise[i]);
}
for (int j = 1; j <= DEFAULT_NOISE_DEQ; j++, i++) {
    if (j == 1)
        pthread_join(noise[i], NULL);
    else
        __VERIFIER_join_symmetric(noise[i]);
}
return 0;
}

```

### H.3 Emptiness client

```

#include <stdio.h>
#include <stdlib.h>
#include <pthread.h>
#include <stdbool.h>
#include <stdatomic.h>
#include <assert.h>

#include "../lib/queue-wrapper.h"

#ifndef MAX_THREADS
# define MAX_THREADS 32
#endif

#ifndef HP_THREAD_LIMIT
# define HP_THREAD_LIMIT 32
#endif

#ifndef N
# define N 2
#endif

queue_t *queue;
queue_t myqueue;
int num_threads;

int __thread tid;

__VERIFIER_hp_t hps[MAX_THREADS + 1][HP_THREAD_LIMIT];
int __thread __hp_index;

void set_thread_num(int i)
{
    tid = i;
}

int get_thread_num()
{
    return tid;
}

__VERIFIER_hp_t *get_free_hp()
{
    int index = __hp_index++;
    assert(index < HP_THREAD_LIMIT);
    return &hps[tid][index];
}

void *thread_n(void *param)
{
    int pid = (intptr_t) param;

    set_thread_num(pid);

    unsigned tmp;

```

```

enqueue(queue, 1);
assert(dequeue(queue, &tmp));
return NULL;
}

int main()
{
    pthread_t threads[N + 1];

    queue = &myqueue;
    num_threads = N;

    init_queue(queue, num_threads);

    for (int i = 0; i < num_threads; i++) {
        if (i == 0)
            pthread_create(&threads[i], NULL, thread_n, (void *) (intptr_t) i);
        else
            threads[i] = __VERIFIER_spawn_symmetric(thread_n, (void *) (intptr_t)
            i, threads[i-1]);
    }

    for (int i = 0; i < num_threads; i++) {
        if (i == 0)
            pthread_join(threads[i], NULL);
        else
            __VERIFIER_join_symmetric(threads[i]);
    }

    return 0;
}

```

## H.4 Mutex client

```

#include <stdlib.h>
#include <pthread.h>
#include <stdatomic.h>
#include <genmc.h>
#include <assert.h>

#include "../lib/lock-wrapper.h"

#ifndef N
# define N 2
#endif

#ifndef M
# define M 1
#endif

int shared;
lock_t lock;

void *thread_n(void *arg)
{
    intptr_t index = ((intptr_t) arg);

    for (int i = 0u; i < M; i++) {
        lock_acquire(&lock);

        shared = index;
        int r = shared;
        assert(r == index);

        lock_release(&lock);
    }
    return NULL;
}

```



```

int main()
{
    pthread_t t[N];

    lock_init(&lock);
    for (int i = 0u; i < N; i++) {
        if (i == 0)
            pthread_create(&t[i], NULL, thread_n, (void *) (intptr_t) i);
        else
            t[i] = __VERIFIER_spawn_symmetric(thread_n, (void *) (intptr_t) i, t[i-1]);
    }
    for (int i = 0u; i < N; i++) {
        if (i == 0)
            pthread_join(t[i], NULL);
        else
            __VERIFIER_join_symmetric(t[i]);
    }

    return 0;
}

```

## H.5 RDCSS client

```

#include <stdio.h>
#include <stdlib.h>
#include <pthread.h>
#include <stdatomic.h>
#include <genmc.h>

#include "rdcss.h"

#ifdef READERS
#define DEFAULT_READERS (READERS)
#else
#define DEFAULT_READERS 0
#endif

#ifdef WRITERS
#define DEFAULT_WRITERS (WRITERS)
#else
#define DEFAULT_WRITERS 0
#endif

#ifdef RDRW
#define DEFAULT_RDWR (RDRW)
#else
#define DEFAULT_RDWR 0
#endif

int readers = DEFAULT_READERS, writers = DEFAULT_WRITERS, rdwr = DEFAULT_RDWR;

_Atomic(value_t) x;
_Atomic(value_t) y;

void *threadW(void *param)
{
    descriptor_t *desc = malloc(sizeof(descriptor_t));
    desc->o1 = MAKE_INT_VAL(0);
    desc->o2 = MAKE_INT_VAL(0);
    desc->n2 = MAKE_INT_VAL(42);
    desc->a1 = &x;
    desc->a2 = &y;

    rdcss(desc);
    return NULL;
}

void *threadR(void *param)
{

```

```
rdcss_read(&y);
return NULL;
}

void *threadRW(void *param)
{
    value_t v = rdcss_read(&y);

    descriptor_t *desc = malloc(sizeof(descriptor_t));
    desc->o1 = MAKE_INT_VAL(0);
    desc->o2 = v;
    desc->n2 = MAKE_INT_VAL(GET_INT_VAL(v) + 1);
    desc->a1 = &x;
    desc->a2 = &y;
    rdcss(desc);
    return NULL;
}

int main()
{
    pthread_t tr[DEFAULT_READERS], tw[DEFAULT_WRITERS], trw[DEFAULT_RDWR];

    for (int i = 0; i < writers; i++) {
        if (i == 0)
            pthread_create(&tw[i], NULL, threadW, NULL);
        else
            tw[i] = __VERIFIER_spawn_symmetric(threadW, NULL, tw[i-1]);
    }
    for (int i = 0; i < readers; i++) {
        if (i == 0)
            pthread_create(&tr[i], NULL, threadR, NULL);
        else
            tr[i] = __VERIFIER_spawn_symmetric(threadR, NULL, tr[i-1]);
    }
    for (int i = 0; i < rdwr; i++) {
        if (i == 0)
            pthread_create(&trw[i], NULL, threadRW, NULL);
        else
            trw[i] = __VERIFIER_spawn_symmetric(threadRW, NULL, trw[i-1]);
    }

    return 0;
}
```

Received 2023-11-16; accepted 2024-03-31