Verifying Read-Copy-Update in a Logic for Weak Memory

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Abstract

Read-Copy-Update (RCU) is a technique for letting multiple readers safely access a data structure while a writer concurrently modifies it. It is used heavily in the Linux kernel in situations where fast reads are important and writes are infrequent. Optimized implementations rely only on the weaker memory orderings provided by modern hardware, avoiding the need for expensive synchronization instructions (such as memory barriers) as much as possible.

Using GPS, a recently developed program logic for the C/C++11 memory model, we verify an implementation of RCU for a singly-linked list assuming "release-acquire" semantics. Although release-acquire synchronization is stronger than what is required by real RCU implementations, it is nonetheless significantly weaker than the assumption of sequential consistency made in prior work on RCU verification. Ours is the first formal proof of correctness for an implementation of RCU under a weak memory model.

Categories and Subject Descriptors D.3.1 [*Programming Languages*]: Formal Definitions and Theory; F.3.1 [*Logics and Meanings of Programs*]: Specifying and Verifying and Reasoning about Programs

General Terms Languages, Theory, Verification

Keywords Concurrency; Weak memory models; C/C++; RCU; Program logic; Separation logic

1. Introduction

Traditionally, most work on concurrent program verification has assumed a *sequentially consistent (SC)* model of memory, in which updates to memory are globally visible to all threads as soon as they occur [10]. For performance reasons, however, modern architectures offer weaker guarantees about the ordering of concurrent memory operations [11, 16]. Although it is possible to simulate SC semantics on such hardware by inserting explicit synchronization instructions (*e.g.,* barriers/fences), the cost of doing so—particularly for high-performance concurrent code—can be prohibitive.

Fortunately, for many concurrent algorithms, full SC behavior is unnecessary, and more limited forms of synchronization suffice. One widely-used example is Read-Copy-Update (RCU) [12, 13]. RCU is a technique, deployed heavily in the Linux kernel, that lets a single writer manipulate a data structure while multiple readers are concurrently accessing it. Instead of directly modifying a piece of the structure, the writer first copies that piece, modifies the copy, and then makes the new copy accessible and the old one inaccessible. Once no readers are capable of accessing the old copy, the writer may safely deallocate it. However, until that time, some readers may see the old copy while others see the new copy, and there is no guarantee when readers will begin to see the new copy.

As this description suggests, RCU employs *some* synchronization (*e.g.,* to ensure memory safety), but *not* full SC semantics, and its reliance on weaker memory assumptions is essential to its efficiency. However, the only existing formal proof of correctness for an RCU-based data structure [7] assumes an SC memory model.

In this paper, we give the first formal proof of correctness for an implementation of RCU under a weak memory model. Specifically, we verify a user-space RCU implementation of linked lists (based on that of Desnoyers et al. [5]), programmed using *release-acquire atomics*, one of the main weak-memory access modes supported by the C/C++11 language standard [8].

Why focus on release-acquire? There are several reasons. First, the semantics of C11's release-acquire mode has been fully formalized [3], rendering our RCU implementation amenable to formal verification, and unlike several other features of the C11 model [20], its semantics is relatively uncontroversial. Second, release-acquire semantics, while significantly weaker than SC, nevertheless provides sufficiently strong synchronization to guarantee safety of our RCU implementation. In fact, release-acquire provides stronger semantics than what real RCU implementations require—the release-consume mode of C11 was designed specifically to support RCU, but the "right" semantics of release-consume is still a matter of debate, and at present most C compilers do not implement it differently from release-acquire [14]. Third, release-acquire semantics is "reasonable", in the sense that one can reason about it using a more restricted version of the kinds of reasoning principles that hold under SC semantics. This claim was substantiated formally by recent work of Turon et al. [17] on a logic called GPS, which supports Hoare-style verification of C11 programs under release-acquire semantics. Here, we leverage (a mild extension of) GPS in our verification, while simultaneously demonstrating a much more significant case study for the use of GPS than any that Turon et al. previously considered.

Above and beyond our formal verification of RCU in GPS (described in full formal detail in our technical appendix [1]), an important contribution of this work is the proof *idea* itself, and it is the elucidation of this proof idea that is our main goal in this paper. Previously, the correctness of RCU has been argued using the concept of a *grace period* during which reader threads may finish accessing an old node before it is deallocated. Indeed, Gotsman et al.'s proof in the SC setting depends on an extension of separation logic with a temporal "since" operator to formalize grace periods. In contrast, our proof avoids any such extension; we rely instead on GPS's notion of *per-location protocols*, which describe how the state of a shared memory location may evolve over time. Using per-location protocols, Turon et al. showed how to formalize

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the folklore intuition that release-writes and acquire-reads support a form of *message passing* between threads. We in turn show how such message passing provides a self-sufficient explanation of how RCU works—*e.g.,* of how the writer tells the readers which nodes have been deallocated, or how the readers tell the writer that they will no longer access them. No additional mechanism is required.

In the rest of the paper, we present the semantics of release-acquire (§2), our implementation of RCU and why intuitively it works (§3), our specification of RCU and why it is useful (§4), a review of GPS with some minor extensions (§5), a high-level description of our verification of RCU in GPS (§6), and discussion of related work (§7).

2. Release-Acquire Semantics

Our implementation of RCU uses a simple imperative while-language extended with C11's release-acquire memory operations. In this section, we try to give some intuition for the semantics of these operations. Thorough, formal presentations of the C11 memory model can be found in Batty et al. [3] and Vafeiadis et al. [20].

The C11 standard divides memory accesses into two types—*atomic* and *non-atomic*—and we will say that a memory location is atomic (resp. non-atomic) if all accesses to it are of that type. Non-atomic accesses are the default variety, appropriate for most use cases: they are fast and do not require the compiler to emit special synchronization instructions, but the standard says that the behavior of a program is undefined if it involves racy non-atomic accesses (*i.e.,* two unordered non-atomic accesses to a single location, at least one of which is a write). Thus, the onus is on the programmer to employ enough synchronization to ensure that there are no non-atomic data races.

One way of implementing such synchronization is using atomic locations, which are *intended* for racy access. The C11 standard lets programmers annotate reads and writes for atomic locations with different consistency level options, ranging from sequentially consistent (SC) to fully relaxed, depending on how cheap they want the accesses to be and how much instruction reordering they can tolerate.

We focus here on only two of these options: *release writes* and *acquire reads*. When a thread performs a release write, and another thread observes that write via an acquire read, the operations that precede the write are guaranteed to "happen-before" the read. This kind of "transitive visibility", as it is often called, allows programmers to use release-acquire to implement a message-passing idiom.

For example, consider the following contrived yet illustrative code (which we will show how to verify in §5):

```
[x]na := 37;                  ||  [y]na := 25;
[lf]rel := 1;                 ||  if ([lf]acq == 1) {
while ([rf]acq != 1) {        ||    [y]na := [x]na;
  /* spin */                  ||  }
}                             ||  [rf]rel := 1;
[x]na := 49;                  ||  /* postcond: y ↪ 37 ∨ y ↪ 25 */
```

Here, we have two non-atomic memory locations, x and y, and two atomic "flags", lf and rf. We write $[x]_{\mathtt{na}}$ to indicate a non-atomic operation on location x, and $[lf]_{\mathtt{rel}}$ and $[lf]_{\mathtt{acq}}$ for release and acquire operations on lf. The code on the sides of the vertical bars represents two different threads, and initially we assume that all locations contain 0.

The effect of this code is to pass control of the non-atomic location x from the left thread to the right thread and back. The left thread initializes location x with value 37, and then sets its flag lf to 1 with a release write, to signal that the right thread can now access x. The right thread checks if lf is set to 1, and if so, it reads the value of x (non-atomically) and sets y to that value; otherwise, it sets y to 25. Because the non-atomic write of 37 to x preceded the release write to lf, and the matching acquire read of lf as 1 (if it occurred) preceded the non-atomic read of x, we will be able to establish: (1) the write to x happened before the read of x, so there is no data race on x, and (2) as a postcondition, y may either point to 25 or 37, but not 0. After the second thread finishes accessing x, it does a release write of 1 to rf to signal to the left thread that it is done. The first thread spins until it observes this write. At this point, it knows it can safely update x again because the second thread's read of x must have happened already.

In the previous example, the two threads synchronized their operations via release writes to the atomic locations lf and rf to send messages back and forth, and acquire reads to receive them. In contrast, here is an example based on the classic "Dekker's algorithm" for mutual exclusion [6], which is safe under SC but *not* under release-acquire:

```
[x]rel := 1                   ||  [y]rel := 1
if [y]acq == 0 then           ||  if [x]acq == 0 then
  [z]na := 1                  ||    [z]na := 2
```

Here, the left thread does a release write to set x to 1, while the right thread does the same for y. Each thread then does an acquire read of the other's variable to see if it has been updated. If not, each thread tries to modify the non-atomic z.

Under an SC semantics, one of the thread's writes must happen before the other: that thread "wins" and may write to z. For instance, if the left thread reads y and sees 0, it concludes that the right thread has not written to y yet, so the left thread knows it has won the race. However, under release-acquire, the writes to x and y are unordered, and it is possible for the left thread to read 0 from y *and* for the right thread to read 0 from x in the same execution. If this happens, they will *both* try to write to z, resulting in a data race.

Informally, if we think in terms of message passing, this example is unsound because it tries to conclude something from the negative fact that a message has *not* yet arrived. To be safe, under release-acquire, we can only draw sound conclusions from the positive information that a message *has* arrived, as in the first example. Later in §5, we will see how this intuitive reasoning is formalized in GPS.

3. RCU

We now describe how RCU can be implemented for a singly linked list using the release-acquire memory operations. In explaining the algorithm, we focus on how the orderings imposed by pairs of release-acquire operations ensure that there are no data races. In each case, we can informally describe these operations in terms of how they send messages between the threads. In §6 our proof will make this message-passing explanation precise.

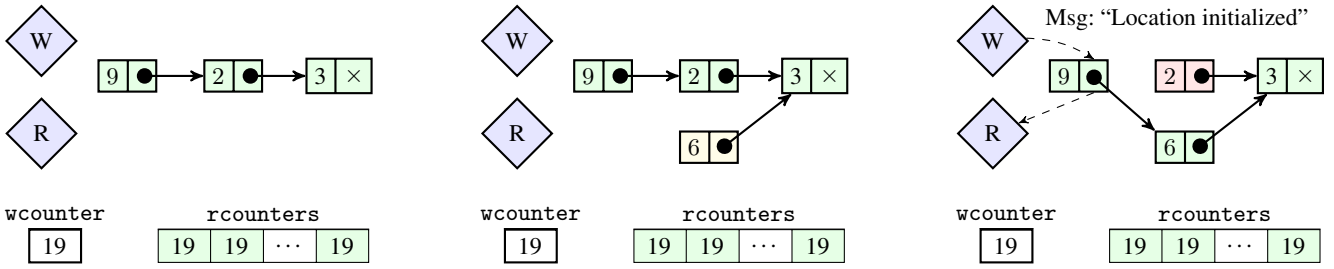
A simplified part of our verified implementation is presented in Figure 1. Nodes in the list are records with two fields. The `data` field contains the contents of the node, and `link` is a pointer to the next node in the list.

Initialization A new RCU instance is created by calling `rcuNew`. This returns a pointer q to the metadata for the RCU instance, which consists of a counter for the writer (q + `wcounter`), an array of counters for the readers (q+`rcounters`, which we describe below), a field containing a pointer to the head of the list (q + `link`), and a pointer to a structure used for a custom allocator that recycles deallocated nodes (q + `free`). The counters all start at 0, and the q + `link` field is initially a null pointer.

Reading The readers access the nodes in the list in a loop that maintains a current pointer into the list. They start the traversal by calling `rcuReadStart` to get the first pointer to the head of the list. This does an acquire read on q + `link` and returns the result.

```
    rcuNew() ≜
1:    let q = alloc(N + 3)
2:    [q + link]_rel := 0;
      for i = 0 to N − 1 do
3:        [q + rcounters + i]_rel := 0;
4:    [q + wcounter]_rel := 0;
5:    [q + free]_na := rcuAllocInit();
6:    q

    rcuReadStart(q) ≜
7:    [q + link]_acq

    rcuReadNext(q, p) ≜
8:    let v = [p + data]_na
9:    let p' = [p + link]_acq
10:   (v, p')

    rcuNodeAppend(q, p, v) ≜
11:   let x = rcuAlloc(q)
12:   [x + data]_na := v;
13:   [x + link]_rel := 0;
14:   [p + link]_rel := x;
15:   x

    rcuNodeUpdate(q, x, p, v) ≜
16:   let c = [x + link]_acq
17:   let x' = rcuAlloc(q)
18:   [x' + data]_na := v;
19:   [x' + link]_rel := c;
20:   [p + link]_rel := x';
21:   rcuSynchronize(q);
22:   rcuFree(q, x);
23:   x'

    rcuNodeDelete(q, x, p) ≜
24:   let c = [x + link]_acq
25:   [p + link]_rel := c;
26:   rcuSynchronize(q);
27:   rcuFree(q, x);

    rcuSynchronize(q) ≜
28:   let oldgc = [q + wcounter]_acq
29:   let newgc = oldgc + 1
30:   [q + wcounter]_rel := newgc;
31:   for i = 0 to N − 1 do
32:     while [q + rcounters + i]_acq != newgc;
33:   end

    rcuQuiescentState(q, tid) ≜
34:   let t = [q + wcounter]_acq
35:   [q + rcounters + tid]_rel := t
```

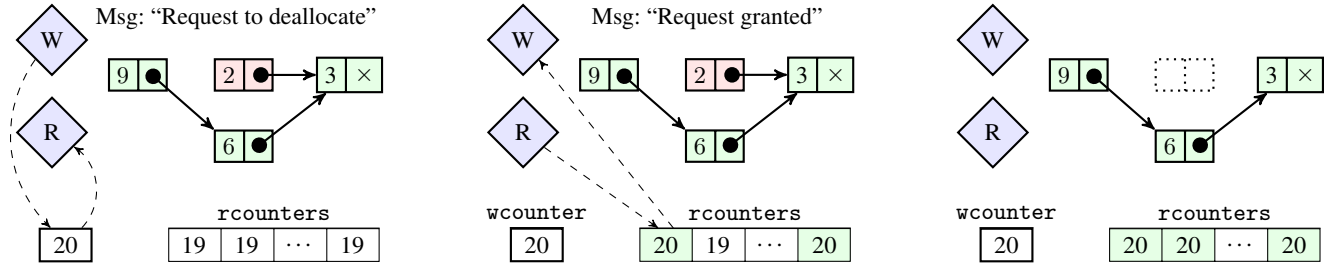
Figure 1. A concurrent linked list with a single writer implemented using QSBR RCU.



(a) State before `rcuNodeUpdate`.

(b) State after the writer executed line 19.

(c) State after the writer linked the new node onto the list (line 20).



(d) State after the writer updated its counter (line 30).

(e) State after the reader has updated its counter (line 35) and the writer noticed it (line 32).

(f) State after `rcuSynchronize`(q) finished. The writer can safely free the node (line 22).

Figure 2. Illustration of updating a node in the list using RCU.

Then, within a loop, they check that their current pointer is not null, and if so, access the value stored at the node and the next node by calling `rcuReadNext` with their current pointer as p. The function simply reads off the `data` and `link` fields of p and returns the results. While the `data` field is read non-atomically, the `link` field is accessed by an acquire read—this ensures correct synchronization with the writer.

Updating the list We now explain how the writer modifies the list by walking through an example shown in Figure 2. It depicts the linked list, as well as the counters in the RCU metadata. The writer thread and one reader thread are represented by diamonds labeled "W" and "R". To represent messages being passed from one thread to the other through a location, we draw a dashed arrow from the sender to the location and another from the location to the reader.

Suppose the writer wants to change the value in the second node of the linked list shown in Figure 2a. To do so, it calls `rcuNodeUpdate`(q, x, p, v), where q is a pointer to the RCU metadata, x is a pointer to the node that it wants to modify, p is a pointer to the previous node, and v is the new value for the node. This function first allocates a new node by calling `rcuAlloc`(q) (not shown in the figure). Next, the writer copies the old node's `link` field, and sets the updated value as in Figure 2b. Then, it updates the previous node's `link` field with a release write so that it points to the new node (line 20), rendering the old node unreachable as shown in 2c. At this point, readers may begin to see the new node when they do an acquire read on the previous `link` pointer (line 9). The pairing between this release write and the readers' acquire reads is the first important point of synchronization in RCU:

Release-Acquire Pair 1 (`link` field): The ordering imposed by the release writes and acquire reads on the `link` fields ensures that the initialization of the node precedes the readers' accesses. In other words, the writer passes a message to the readers saying that the next node is safe to access.

Similar synchronization points occur when writers append new nodes onto the end of the list with `rcuNodeAppend` or delete a node from the list with `rcuNodeDelete`.

Deallocating the old node After completing the release write in Figure 2c, the writer calls `rcuSynchronize` to wait until no readers can access the old copy any longer, so that it can deallocate the removed node. There are a number of ways to implement `rcuSynchronize` without sacrificing reader performance. The code in Figure 1 uses Quiescent State Based Reclamation (QSBR) [5].

In QSBR, the writer begins the synchronization operation by incrementing its counter (line 30 and Figure 2d). It then repeatedly reads each reader counter in turn until they all match the writer counter's new value. When readers are not accessing the list (that is, they are *quiescent*), they periodically call `rcuQuiescentState`, which examines the writer's counter and copies its value into the reader's counter (Figure 2e). Once the writer sees that every reader's counter matches its own, it knows they have all entered a quiescent state since the old node became unreachable. This means that if the readers access the list in the future, they will not access the old node, so the node can be safely deallocated (Figure 2f).

These counter fields must be atomic, because the readers will try to concurrently read the writer's counter as the writer is incrementing it, and vice-versa. Both counters are involved in a release-acquire synchronization:

Release-Acquire Pair 2 (`wcounter` field): The synchronization between the write on line 30 and the read on line 34 guarantees that once the reader sees the updated counter, it will see the update that made the old node unreachable (line 20). When the writer increments its counter, it publishes the fact that a node has been made unreachable together with a request for permission to deallocate the node.

Release-Acquire Pair 3 (`rcounters` + tid field): When the readers update their counters to match the writer's on line 35, they acknowledge the writer's request by giving up their own permission to access the unreachable node. The release-acquire ordering ensures that any accesses the reader was doing before calling `rcuQuiescentState` all finish before the writer proceeds to deallocate the node.

Memory management After calling `rcuSynchronize`, the writer calls `rcuFree` (not shown in Figure 1; see the appendix [1]). Earlier work on formally specifying the C11 memory model [3] did not address the semantics of `free`. Since our focus is on RCU rather than the behavior of deallocation in C11, we have opted to remain within the scope of what we can formalize—we thus hand-roll our own naive, *ad hoc* memory reclamation routine in `rcuFree`. The call to `rcuFree` adds the address of the old node to a pool. The implementation of `rcuAlloc` (again, see the appendix) first tries to remove an address from the pool and return it. If the pool is empty, it calls `alloc`().

In this simplified version of our implementation, there is a fixed number of readers, N, and the writer immediately synchronizes and deallocates the old node as soon as it performs an update. In the full version verified in the appendix, we allow the readers to register themselves dynamically and let the writer batch its deallocations for efficiency.

$\{\mathsf{true}\}$
`rcuNew`()
$\left\{q.\, \exists H.\, \mathsf{WriterSafe}(q, [(q, \mathsf{null})]) * \mathop{\Large *}_{tid<N} \mathsf{ReaderSafe}(q, H, tid)\right\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L')\}$
$[p + \texttt{link}]_{\texttt{acq}}$
$\left\{\begin{array}{l} p'.\, \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L') * ((p' = 0 \wedge L' = \mathtt{nil}) \\ \quad \vee (p' \neq 0 \wedge \exists L'', v'.\, L' = (p', v') \cdot L'')) \end{array}\right\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L') \wedge v \neq \mathsf{null}\}$
$[p + \texttt{data}]_{\texttt{na}}$
$\{x.\, x = v \wedge \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L')\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v)) * \square P(v')\}$
`rcuNodeAppend`(q, p, v')
$\{x.\, \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot (x, v'))\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L') * \square P(v_1')\}$
`rcuNodeUpdate`(q, x, p, v_1')
$\{x'.\, \mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x', v_1') \cdot L')\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L')\}$
`rcuNodeDelete`(q, x, p)
$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot L')\}$

$\{\mathsf{ReaderSafe}(q, H, tid)\}$
`rcuReadStart`(q)
$\{p.\, \mathsf{ReaderSafe}(q, H, tid) * \square\mathsf{SafePtr}(q, H, p)\}$

$\{\mathsf{ReaderSafe}(q, H, tid) * \square\mathsf{SafePtr}(q, H, p) * p \neq 0\}$
`rcuReadNext`(q, p)
$\{(v, p').\, \mathsf{ReaderSafe}(q, H, tid) * \square\mathsf{SafePtr}(q, H, p') * \square P(v)\}$

$\{\mathsf{ReaderSafe}(q, -, tid)\}$
`rcuQuiescentState`(q, tid)
$\{\exists H'.\, \mathsf{ReaderSafe}(q, H', tid)\}$

Figure 3. Specifications of the RCU operations.

4. RCU Specification

GPS [17] lets us prove Hoare-style triples of the form:

$$\{P\}\ e\ \{x.\, Q\}$$

asserting that if a thread starts with the resources described by P and executes expression e, then:

- The execution of e is guaranteed to be free of memory errors (e.g. accessing uninitialized data) and non-atomic data races.
- If e terminates with value V, then $[V/x]Q$ describes the thread's resources afterward.

Later, we will review the logical mechanisms that GPS provides for proving these triples. For now, we describe the specification for RCU that we will prove. The full specification is shown in Figure 3. We assume some fixed predicate $P(x)$ that we require to hold of values stored in the list. Any value inserted by the writer must satisfy this predicate, and readers are guaranteed that values they get out will also satisfy it. The RCU specification then employs three predicates which are defined in terms of underlying GPS primitives but can be treated abstractly by a client: $\mathsf{WriterSafe}(q, L)$, $\mathsf{ReaderSafe}(q, H, tid)$, and $\mathsf{SafePtr}(H, p)$.

$\mathsf{WriterSafe}(q, L)$ represents the permissions owned by the writer. The logical list L is of the form $(q, \mathsf{null}) \cdot (l_1, v_1) \cdot$

$(l_2, v_2) \cdots (l_n, v_n)$, where l_i is a pointer to the ith node in the list, and v_i is the value stored in the `data` field of that node. The predicate says that for the RCU structure with metadata at q, the physical list contains the nodes mentioned in L. We generate this permission when we create a new RCU instance, at which point L consists only of (q, null). Accessing the `link` field of a pointer in L just returns the next pointer in L. Each of the writer's methods consumes this permission, and returns a version where the contents of L have been modified accordingly.

$\mathsf{ReaderSafe}(q, H, tid)$ is the analogous permission for readers. From the perspective of the client code, H is completely abstract: it simply represents the version of the list that the tid-th reader sees. $\mathsf{SafePtr}(q, H, p)$ means that p is a pointer to a properly initialized node. The specification for `rcuReadStart` says that it always returns a SafePtr. As the reader inspects the list using `rcuReadNext`, p must be a non-null SafePtr, and when the call returns, it returns another SafePtr.

When the reader calls $\texttt{rcuQuiescentState}(q)$, it gives up its current $\mathsf{ReaderSafe}(q, H, tid)$ and receives $\mathsf{ReaderSafe}(q, H', tid)$ in return, for some fresh H'. This makes any previous SafePtr assertions unusable, and forces the reader to start again at the head of the list by getting a new SafePtr from `rcuReadStart`.

Finally, note that some predicates (P and SafePtr) are "boxed", *i.e.,* appearing under a $\Box$ modality. This means that these predicates denote "duplicable facts" (with the property that $\Box Q \Leftrightarrow \Box Q * Q$) as opposed to uniquely owned permissions, a distinction that will be explored further in the next section.

5. GPS

In this section, we briefly review some of the key mechanisms in GPS that we will use in verifying our RCU implementation. We then illustrate their use on the simple message-passing example from §2. Although the example is contrived, its verification closely mirrors the structure of the RCU verification, and it shows off all the features of GPS working in tandem. It is thus quite useful as a warm-up for the main attraction.

5.1 Key Features of GPS

The four key features of GPS are as follows.

Ownership of non-atomics The assertion $x \hookrightarrow v$ says that x is a non-atomic location pointing to the value v. This assertion is precisely the standard points-to assertion of separation logic [15]: whoever asserts $x \hookrightarrow v$ is the exclusive "owner" of x, and has the freedom to read and write it arbitrarily.

Here, we also extend GPS slightly to support *fractional permissions* [4] on non-atomic locations. We annotate the points-to relation with a permission k, which is an element of a permission algebra [18]. This algebra is a set with a distinguished element $\top$, representing "full" permission, and a partial operation $\oplus$ for combining permissions. Now, $x \overset{k}{\hookrightarrow} v$, where $k \neq \top$, denotes only ownership of a partial permission to access x, which means the ability to read x but not write it. The initial (full) owner of x may thus split up its ownership assertion into pieces to be given out to readers, and then later on collect those pieces to reconstitute the full permission so that it can update x. Crucially, though, with neither full nor fractional ownership is it possible for one thread to read x at the same time another may be writing it: thus, we guarantee absence of data races on non-atomics.

In the RCU proof, since we assume one writer and a fixed number of readers, N, our permission algebra will be sets of thread IDs, with $\top = \{0, \ldots, N\}$ and $\oplus$ defined as disjoint set union. We write $x \overset{tid}{\hookrightarrow} v$ (for $0 \leq tid \leq N$) as shorthand for $x \overset{\{tid\}}{\hookrightarrow} v$, the partial permission for thread tid to read x (thread N is the writer).

Protocols for message passing via atomics Unlike non-atomics, atomic locations are meant to be read and written simultaneously. We therefore cannot make any stable assertions about the precise contents of an atomic location, but we *can* assert something about how those contents are permitted to evolve over time. We call such an assertion a *protocol* assertion, $\boxed{x : s \mid \tau}$. It asserts two things. First, it says that x is governed by the protocol τ. This protocol consists of a partially ordered set of logical *states* S that x can be in, together with an *interpretation* function $\tau(s, v)$ that says what assertion must hold when x is in logical state $s \in S$ and stores value v. Second, the protocol assertion says that x is *at least* in state s of its protocol. This assertion is a duplicable fact, and may thus be shared freely between threads, because GPS requires writes to x to always *advance* the state of its protocol—so once x is at least in state s, it will remain so forever.

Through their interpretation functions, protocols offer a way for threads to pass messages to each other. Specifically, suppose two threads both know $\boxed{x : s \mid \tau}$. When one of the threads writes v to x, it must be able to prove that $\tau(s', v)$ holds for some future state s' of s. Subsequently, when the other thread performs a read on x, observing value v, it will learn that there is some future state s' of s such that $\tau(s', v)$ holds. The protocol has thus served to transmit the knowledge of $\exists s' \sqsupseteq s.\ \tau(s', v)$ from one thread to the other.

Exchanges for ownership transfer While protocols support the transfer of knowledge (*i.e.,* duplicable facts) between threads, *exchanges* support the transfer of *exclusive ownership* of resources between them.[1] This will be very important when verifying our message-passing example (see §5.2 below), wherein we want to pass exclusive ownership of $x \hookrightarrow 37$ back and forth between the two threads.

The exchange mechanism is very simple. Suppose P and Q are assertions such that $P * P \Rightarrow \mathsf{false}$ and $Q * Q \Rightarrow \mathsf{false}$, *i.e.,* they denote exclusive ownership, so two threads cannot assert P simultaneously (and likewise for Q). We write $\sigma : P \leftrightsquigarrow Q$ to say that σ is the name of an exchange between P and Q, and we write $\mathsf{exch}(\sigma)$ to represent the assertion that the exchange σ has been created. The idea is that σ, once created, represents an invariant governing some shared state, which asserts that that shared state *either* satisfies P or it satisfies Q. Once created, the σ invariant is enforced permanently, and thus the assertion $\mathsf{exch}(\sigma)$ is duplicable knowledge that can be freely shared amongst threads.

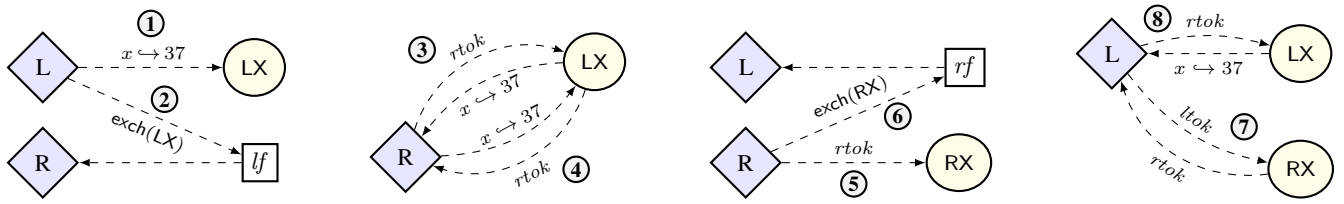
To see how exchanges support ownership transfer, suppose thread 1 owns P, thread 2 owns Q, and thread 1 wishes to transfer ownership of P to thread 2. Thread 1 can create the exchange σ by giving up ownership of P to the exchange, thereby learning $\mathsf{exch}(\sigma)$ in return. It may then use release-acquire message passing (as described above) to inform thread 2 of the knowledge that σ exists. Since thread 2 owns Q, it can then give up Q in exchange for P. These logical ownership transfers are summarized as follows:

$$(P \vee Q) \Rrightarrow \mathsf{exch}(\sigma) \quad P \wedge \mathsf{exch}(\sigma) \Rrightarrow Q \quad Q \wedge \mathsf{exch}(\sigma) \Rrightarrow P$$

Note that the assumption that assertions P and Q are exclusive (non-duplicable) is essential in order to ensure that there is a *unique* recipient of the ownership transfer. For instance, if Q were some duplicable fact, then multiple threads would be able to exchange Q for P, which would result (unsoundly) in multiple threads gaining simultaneous ownership of P.

Ghost PCMs for encoding auxiliary state Ghost (or auxiliary) state is a ubiquitous mechanism in program logics, enabling the verifier to record and manipulate additional *logical* state beyond the physical state manipulated by the program itself. GPS supports a

[1] The original version of GPS featured a slightly more limited primitive called *escrows*. Exchanges generalize escrows to support bidirectional transfer.



(a) The left thread creates and publishes the exchange LX.

(b) The right thread uses the LX exchange twice.

(c) The right thread creates and publishes RX.

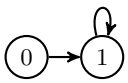
(d) The left thread uses LX and RX to get $x \hookrightarrow 37$.

Figure 4. Message passing and ownership transfer in the simple message-passing example.

$\mathsf{LX} : x \hookrightarrow 37 \leftrightsquigarrow \boxed{rtok : \diamond\ \mathsf{Tok}}$

$\mathsf{RX} : \boxed{rtok : \diamond\ \mathsf{Tok}} \leftrightsquigarrow \boxed{ltok : \diamond\ \mathsf{Tok}}$

lf, rf:



$\mathsf{LFP}(s, v) \triangleq (s = 0 * v = 0) \vee (s = 1 * v = 1 * \mathsf{exch}(\mathsf{LX}))$

$\mathsf{RFP}(s, v) \triangleq (s = 0 * v = 0) \vee (s = 1 * v = 1 * \mathsf{exch}(\mathsf{RX}))$

Figure 5. Protocols/exchanges for message-passing example.

very general notion of ghost state in the form of user-defined *partial commutative monoids (PCMs)*. Given a PCM μ and an element $t \in \mu$ we write $\boxed{\gamma : t\ \mu}$ to say that a thread owns element t from instance γ of the monoid μ. Then, we can split or combine ghost state elements as follows:

$$\boxed{\gamma : t \cdot_\mu t'\ \mu} \quad \Leftrightarrow \quad \boxed{\gamma : t\ \mu} * \boxed{\gamma : t'\ \mu}$$

In particular, if $t \cdot_\mu t'$ is not defined (which is possible since the monoid is partial), then $\boxed{\gamma : t\ \mu} * \boxed{\gamma : t'\ \mu} \Rightarrow \mathsf{false}$.

Recent work has shown that PCMs are remarkably expressive [9]. In this paper, we focus on two relatively simple types of PCMs that are relevant to the RCU proof: the *permission token* and *master/snapshot* PCMs.

Permission tokens represent capabilities to perform certain operations. We will use them, for instance, to represent the permissions to make certain steps in a protocol, or the permission to access certain exchanges. Permission tokens are defined by the monoid Tok which has two elements $\diamond$ and ϵ, with ϵ as identity and $\diamond \cdot \diamond$ undefined. The key property of a permission token is that it is non-duplicable ($\boxed{\gamma : \diamond\ \mathsf{Tok}} * \boxed{\gamma : \diamond\ \mathsf{Tok}} \Rightarrow \mathsf{false}$) and thus represents an exclusive capability. We discuss master/snapshot PCMs in §6.1.

5.2 Verifying the Message-Passing Example

To show how the above mechanisms work together, let us return to the first example in §2. Our verification, which we describe here at a high (but still detailed) level, guarantees two things: (a) the postcondition, namely that, once the threads terminate, y points to 25 or 37, and (b) that the code is "safe", meaning that there are no data races on the non-atomic x and y.

```
[x]na := 37;                    ||  [y]na := 25;
[lf]rel := 1;                   ||  if ([lf]acq == 1) {
while ([rf]acq != 1) {          ||    [y]na := [x]na;
  /* spin */                    ||  }
}                               ||  [rf]rel := 1;
[x]na := 49;                    ||  /* postcond: y ↪ 37 ∨ y ↪ 25 */
```

We walk through the proof now step by step. These steps are illustrated pictorially in Figure 4, and they involve protocols and exchanges that are defined formally in Figure 5.

At the start of the proof, we associate the flags lf and rf with the left and right flag protocols **LFP** and **RFP**, respectively (explained below). We also create the left and right permission tokens, $\boxed{ltok : \diamond\ \mathsf{Tok}}$ and $\boxed{rtok : \diamond\ \mathsf{Tok}}$, and give the left and right threads exclusive ownership of their respective tokens.

Step 1 (Fig. 4a): The left thread first sets x to 37. It then wants to transfer ownership of x to the right thread. To do so, it creates the exchange LX. By giving up ownership of $x \hookrightarrow 37$ to the exchange, it gains the knowledge exch(LX) that LX exists.

Step 2 (Fig. 4a): The left thread now wants to send its knowledge of exch(LX) to the right thread by setting its flag, lf, to 1. To reason about this, we use the left flag protocol **LFP**. This protocol asserts that x is initially 0, and that it may be set to 1 but can never be set back to 0 again. It also asserts that when lf is set to 1, it must be the case that exch(LX) holds. Since the left thread knows exch(LX), it is free to update lf to 1 (updating the logical state s of lf's **LFP** protocol to 1 as well).

Step 3 (Fig. 4b): The right thread may or may not observe that lf has been set to 1. In case it does not observe it, this and the next step are skipped. In case it *does* observe it, it learns that the **LFP** protocol must be in the 1 state, and hence it learns that LX exists. It then uses LX to exchange its own permission token, $rtok$, for ownership of $x \hookrightarrow 37$. Now that it owns x, it can safely read it and be sure that it will see the value 37.

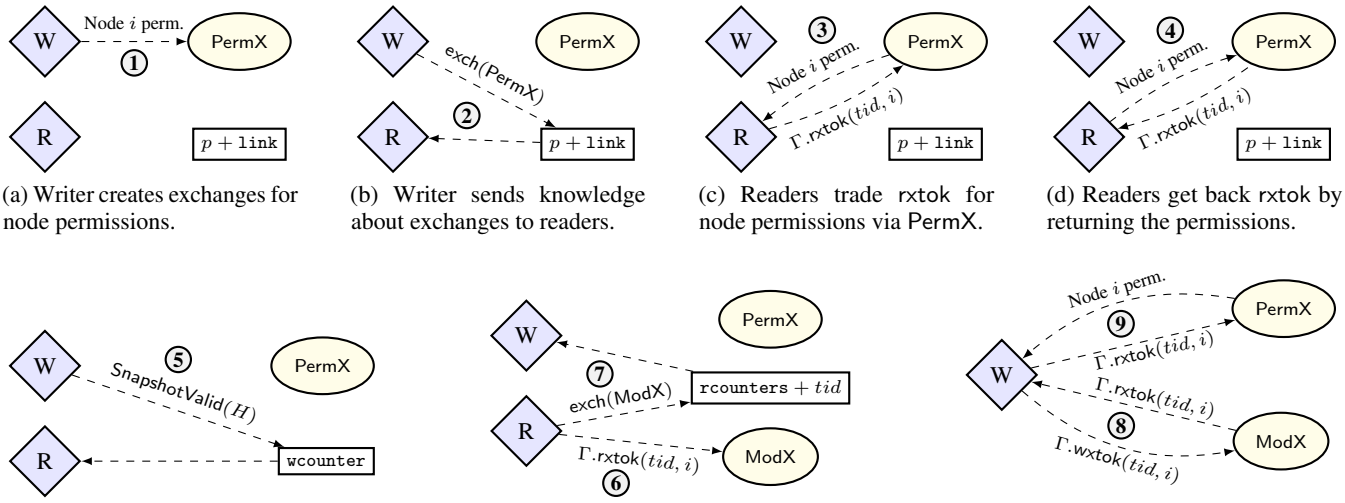
Step 4 (Fig. 4b): The right thread now wants to transfer ownership of x back to the left thread. To achieve this, its first step is to perform the reverse trade on LX, putting ownership of $x \hookrightarrow 37$ back under control of LX in return for its permission token $rtok$. **Note**: at this point, regardless of whether Steps 3 and 4 were performed or not, y points to either 25 or 37, as desired.

Step 5 (Fig. 4c): The right thread next creates the exchange RX by transferring its permission token $rtok$ into the exchange. In doing so, it learns exch(RX).

Step 6 (Fig. 4c): The right thread now wants to send its knowledge of exch(RX) to the left thread by setting its flag, rf, to 1. To reason about this, we use a right flag protocol, **RFP**, that is very similar to the left flag protocol, **LFP**, the only difference being that in state 1, **RFP** asserts exch(RX) (rather than exch(LX)). The right thread may thus set rf to 1 because it knows RX exists.

Step 7 (Fig. 4d): The left thread loops until it observes that rf has been set to 1. Once it observes this, it knows that the **RFP** protocol must be in state 1 and thus that RX exists. It then uses RX to exchange its own permission token, $ltok$, for the right permission token, $rtok$.

Step 8 (Fig. 4d): Finally, the left thread uses its original LX exchange to trade the right permission token, $rtok$, for ownership of $x \hookrightarrow 37$. It now knows that it has exclusive ownership of x and may therefore safely modify it again.



(a) Writer creates exchanges for node permissions.

(b) Writer sends knowledge about exchanges to readers.

(c) Readers trade rxtok for node permissions via PermX.

(d) Readers get back rxtok by returning the permissions.

(e) Writer requests deallocation permission by sending the list snapshot.

(f) Readers create exchange for requested rxtok and notify the writer.

(g) Writer uses ModX and PermX to retrieve the node permissions.

Figure 6. Message passing and ownership transfer in our RCU implementation.

6. RCU Proof Overview

In §5, we saw how protocols and exchanges could be used to implement message passing and ownership transfer. We now use these mechanisms to formalize the intuitive explanation we gave for RCU in §3.

There are two important ownership transfers involved in RCU: the writer transfers fractional ownership of nodes to readers when the nodes are added to the list, and readers transfer the fractional ownership of deleted nodes back to the writer during synchronization. The astute reader may note, however, that these nodes consist of both a non-atomic (`data`) field and an atomic (`link`) field, but in §5 we only discussed fractional ownership of non-atomics. Indeed, what does it even mean to "own" an atomic location, given that protocol assertions on atomic locations are duplicable?

We will return to this subtlety in §6.1; first, we will explain at a high level how protocols and exchanges are used in the steps of the algorithm, glossing over the details of ownership for atomics. Figure 6 shows the message passing and ownership transfer involved in the release-acquire pairs in terms of the predicates and exchanges used in the proof. Figure 7 contains the formal definitions. Note that these definitions refer to various pieces of ghost state (*e.g.,* tokens) projected from Γ. This Γ is just a record collecting together all the state associated with a particular instance of an RCU linked list.

Step 1 (Fig. 6a): After initializing a new node with value v at physical location x, the writer will own $x + \texttt{data} \hookrightarrow v$, as well as the $x + \texttt{link}$ field. Since in our RCU implementation it is possible that the physical x is a recycled node (*i.e.,* one that participated in the data structure previously but was deallocated and reallocated), we also create a fresh *abstract node ID*, i, which serves as a logical proxy for the *current* allocation of x. (Each time x is re-allocated, it will thus be associated with a different abstract ID. This simplifies protocol reasoning, enabling us, for instance, to use one-time token permissions to pass ownership of x back and forth between writer and readers, even though the physical x may in fact be passed back and forth multiple times if it is recycled.) This ID i will designate a token that a reader will have to use to get access to the node. The writer then splits the ownership of $x + \texttt{data}$ and $x + \texttt{link}$ into fractional pieces for the readers. For each reader thread $tid < N$, it transfers the fractional pieces designated for reader tid into an exchange, $\mathsf{PermX}(\Gamma, x, tid, i)$. The other side of this exchange is the (tid, i) token from the $\Gamma.\mathsf{rxtok}$ ghost state. Reader tid begins by owning all of the $\{tid\} \times \mathbb{N}$ of these tokens. (Compare this with the LX exchange created in Step 1 of the example in §5.2.)

Step 2 (Fig. 6b): We set up a protocol **LLP** on the `link` field, which formalizes Release-Acquire Pair 1 from §3. When the writer updates the `link` field of the parent p to point to x, it will store the knowledge that each $\mathsf{PermX}(\Gamma, x, tid, i)$ exchange has been created. (Compare this with **LFP** in Step 2 in §5.2.)

Step 3 (Fig. 6c): When reader tid reads $p + \texttt{link}$, it will learn about $\mathsf{PermX}(\Gamma, x, tid, i)$, and use its $\Gamma.\mathsf{rxtok}$ token to get access to x's fields.

Step 4 (Fig. 6d): When the reader is done with the node, it uses PermX in the opposite direction to get its $\Gamma.\mathsf{rxtok}$ token back. (Compare this and the previous step with Steps 3 and 4 in §5.2.)

Step 5 (Fig. 6e): Now, suppose later on the writer has deleted the node at location x, where x is associated with abstract node ID i, and now the writer wants to deallocate it. To do so, it increments `wcounter`, which in turn is governed by protocol **WCP** (formalizing Release-Acquire Pair 2 from §3). It stores $\mathsf{SnapshotValid}(H)$, which asserts that the abstract IDs for the nodes in the list are in fact in the state suggested by the "history snapshot" H. We explain history snapshots in §6.1, but intuitively, they represent the history of updates to the list, and H here is the most up-to-date history. In particular, since x has been deleted from the list, H here will mark x as a dead node. When reader tid sees the updated writer's counter, it infers that the writer wants to deallocate x because H marks x as dead.

Step 6 (Fig. 6f): For each of the abstract nodes i that the writer has requested for deallocation, the reader creates a $\mathsf{ModX}(\Gamma, tid, i)$ exchange, into which it transfers its (tid, i)-th $\Gamma.\mathsf{rxtok}$. The other side of the exchange is a corresponding (tid, i) token from $\Gamma.\mathsf{wxtok}$. Here, $\Gamma.\mathsf{wxtok}$ is a set of tokens that the writer starts with, which it uses to retrieve the reader's tokens. (Compare with the creation of the RX exchange in Step 5 in §5.2.)

Step 7 (Fig. 6f): The reader transmits its knowledge of the existence of these ModX exchanges by updating its counter, $\texttt{rcounters} + tid$. This counter is in turn governed by protocol $\mathbf{RCP}(\Gamma, tid)$,

$$\mathsf{PermX}(\Gamma, l, tid, i) : \Big((\exists v.\, l + \texttt{data} \overset{tid}{\hookrightarrow} v * P(v)) * (\exists j, L.\, \boxed{l + \texttt{link} : (i \cdot L, -) \mid \mathbf{LLP}(\Gamma, l, j)} * \boxed{j : \mathrm{Master}_{tid}(i \cdot L)}\Big)$$
$$\rightsquigarrow \boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}}$$

$$\mathsf{ModX}(\Gamma, tid, i) : \boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}} \rightsquigarrow \boxed{\Gamma.\mathsf{wxtok} : \{(tid, i)\}}$$

$$\mathsf{SnapshotValid}(\Gamma, H) \triangleq H \neq \texttt{nil} * \boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H)} * \mathsf{base}(H) \notin \mathsf{dead}(H) * H_*(\Gamma.q) = \mathsf{base}(H) \cdot \texttt{nil}$$
$$* \ (\forall l \in \mathrm{dom}(H_*).\, \exists j.\, \boxed{j : \mathrm{Snapshot}(H_*(l))} * \boxed{l + \texttt{link} : - \mid \mathbf{LLP}(\Gamma, l, j)}$$
$$* \ H^*(\mathsf{hd}(H_*(l))) \neq \top \Rightarrow \boxed{l + \texttt{link} : (H_*(l), H^*(\mathsf{hd}(H_*(l)))) \mid \mathbf{LLP}(\Gamma, l, j)})$$

Protocol	**State**	**Interpretation** (where x is the value stored at the location in question)	**Ordering** (State $\leq$ State$'$)
$\mathbf{LLP}(\Gamma, l, j)$	$(i_0 \cdot L_0,$ $i_1 \cdot L_1)$	$(i_1 \neq \mathsf{null} \Rightarrow x \neq 0 * H_*(x) = i_1 \cdot - * \forall t < N.\, \mathsf{exch}(\mathsf{PermX}(\Gamma, x, t, i_1)))$ $* \ (i_1 = \mathsf{null} \Rightarrow x = 0) * \exists H.\, \boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H)}$ $* \boxed{j : \mathrm{Snapshot}(i_0 \cdot L_0)} * H^*(i_0) = i_1 \cdot L_1 * H_*(l) = i_0 \cdot L_0$	Lexicographic, with $L_0 \leq L_0'$ if L_0 is a suffix of L_0'
$\mathbf{WCP}(\Gamma)$	(H, v)	$x = v * \boxed{\Gamma.\mathsf{ctok} : \{(N, v)\}} * \mathsf{SnapshotValid}(\Gamma, H)$	$(H = H' \wedge v \leq v')$ $\vee \ (H \leq H' \wedge v < v')$
$\mathbf{RCP}(\Gamma, tid)$	(H, v)	$x = v * \boxed{\Gamma.\mathsf{ctok} : \{(tid, v)\}} * (\forall i \in \mathsf{dead}(H).\, \mathsf{exch}(\mathsf{ModX}(tid, i)))$ $* \boxed{\Gamma.q + \texttt{wcounter} : (H, v) \mid \mathbf{WCP}(\Gamma)}$	Same as $\mathbf{WCP}(\Gamma)$

Figure 7. Exchanges and protocols for RCU.

formalizing Release-Acquire Pair 3 from §3. (Compare with the use of protocol **RFP** in Step 6 in §5.2.)

Step 8 (Fig. 6g): As the writer sees the updated $\texttt{rcounters} + tid$ fields, it uses each $\mathsf{ModX}(tid, i)$ it learns about to exchange its own (tid, i)-th $\Gamma.\mathsf{wxtok}$ token for the corresponding (tid, i)-th $\Gamma.\mathsf{rxtok}$ token. (Compare with the token exchange that occurs in Step 7 in §5.2.)

Step 9 (Fig. 6g): Finally, it uses these $\Gamma.\mathsf{rxtok}$ tokens with the $\mathsf{PermX}(\Gamma, x, tid, i)$ exchange to get back all the fractional permissions for x. After it has done this for for every reader's token, it will have collected the full permission for x, and it may deallocate the node. (Compare with the final Step 8 in §5.2.)

In the remainder of this section, we first present some more detail about the ghost state constructions needed in the proof, including those needed to account for ownership transfer of atomics (§6.1). We then explain the definitions of the abstract predicates ReaderSafe and SafePtr (from the spec in Figure 3) and sketch why the reader specifications are correct (§6.2). We conclude with a brief discussion of the extensions to our basic RCU implementation that are supported by our full verification (§6.3). The definition of WriterSafe and the full Hoare-style proofs are given in the appendix.

6.1 Ghost State

Our proof uses ghost state in three ways: (1) as permission tokens for exchanges, (2) to control the progress of protocols, and (3) to track the state (and more generally the history) of the linked list.

Exchange tokens We have the $\Gamma.\mathsf{rxtok}$ and $\Gamma.\mathsf{wxtok}$ tokens for the PermX and ModX exchanges. As we want a fresh token for each thread and for each abstract node ID, we take the PCM to be the powerset of $\{0, \ldots, N-1\} \times \mathbb{N}$ with disjoint union as composition. Reader tid starts with the set $\{tid\} \times \mathbb{N}$ of $\Gamma.\mathsf{rxtok}$. Meanwhile, the writer starts with all of the $\Gamma.\mathsf{wxtok}$.

Protocol state tokens Each thread has a counter which it alone is allowed to modify. The way we enforce this is by giving the thread a set of tokens, one for each state in the protocol associated with the counter. The interpretation function for the protocol then requires that to move to state s, the thread must give up the token which matches s. The thread begins with all of these tokens and deposits one each time it updates its counter. It knows that no other thread could have concurrently updated its counter, because it owns the unique token needed for the update.

For RCU, we use the powerset of $\{0, \ldots, N\} \times \mathbb{N}$ PCM for these tokens. The instance of this PCM is called $\Gamma.\mathsf{ctok}$ (for "counter token"). Reader tid starts with $\{tid\} \times \mathbb{N}$, and the writer starts with $\{N\} \times \mathbb{N}$. Then, we set up the interpretations of the **WCP** and **RCP** protocols for the counters so that each counter can only be updated to value v by the thread tid holding the appropriate counter token.

Master/snapshot PCM We will use a particular PCM construction to track the history of various objects in the RCU proof. The construction is a variant of the *authoritative monoid* described in Jung et al. [9]. This PCM allows a thread to update the history of an object by extending a non-duplicable "master" view of it. The PCM will also contain duplicable elements called "snapshots", which are partial, possibly stale, histories of the object. Readers use knowledge of these snapshots to establish lower bounds on the object's state.

Suppose P is a poset that represents a state transition system for some object. Suppose further that P has a least element, as well as an additional ordering property that for all $x, y, z \in P$, if $x \leq z$ and $y \leq z$, then either $x \leq y$ or $y \leq x$. We can then define a PCM whose elements have the form $\mathrm{Master}_k(p)$ and $\mathrm{Snapshot}(p)$, where $p \in P$ and k is a partial permission. Composition for this PCM is defined as follows (if the r.h.s. is undefined, so is the composition):

$$\mathrm{Master}_k(p) \cdot \mathrm{Master}_{k'}(p') \triangleq \mathrm{Master}_{k \oplus k'}(p), \text{ if } p = p'$$
$$\mathrm{Snapshot}(p) \cdot \mathrm{Master}_k(p') \triangleq \mathrm{Master}_k(p'), \text{ if } p \leq p'$$
$$\mathrm{Master}_k(p) \cdot \mathrm{Snapshot}(p') \triangleq \mathrm{Master}_k(p), \text{ if } p' \leq p$$
$$\mathrm{Snapshot}(p) \cdot \mathrm{Snapshot}(p') \triangleq \mathrm{Snapshot}(\max(p, p'))$$

We will write $\mathrm{Master}(p)$ as an abbreviation for $\mathrm{Master}_\top(p)$ (the full master permission).

To see why this construction is useful, imagine the RCU writer owns $\mathrm{Master}(p)$. This enables the writer to do two things. First, owning $\mathrm{Master}(p)$ entitles the writer to update it to any $\mathrm{Master}(p')$ such that $p' \geq p$. Formally, this is justified by GPS's "frame-preserving ghost update rule", which says that the update is valid so long as any PCM elements compatible with $\mathrm{Master}(p)$ are also compatible with

Master(p'). This "frame-preserving" condition guarantees that the writer's update does not invalidate the knowledge of other threads, and it holds here because indeed the only snapshots Snapshot(p'') compatible with Master(p) must have $p'' \leq p \leq p'$. Second, since Master(p) = Master(p) $\cdot$ Snapshot(p), owning Master(p) entitles the writer to fork off as many copies of Snapshot(p) as needed and transmit knowledge of them to readers through protocols. If a reader learns of Snapshot(p) through such a protocol, it then knows that p is a lower bound on the state of the object, *i.e.,* that the master copy must be in a state $p' \geq p$, and that if it ever learns of some other Snapshot(p'), it must be that either $p \leq p'$ or $p' \leq p$.

We will instantiate this definition with two different posets in the proof: the poset of *action histories*, which track the sequence of actions taken by the writer, and the poset of *abstract node ID histories*, which track the connection between a physical location and its logical proxies.

Action histories As part of Release-Acquire Pair 2, the writer needs to inform the readers that the node it wants to deallocate is no longer reachable. To do this, we record the history of the list as a piece of ghost state H, which is a list of abstract *actions* taken by the writer. Actions are of the form $\texttt{alloc}(l, i, i')$, $\texttt{upd}(i, i')$, or $\texttt{del}(i)$, where l is a location, $i \in \mathbb{N}$ and $i' \in \mathbb{N} \cup \{\mathsf{null}\}$. An $\texttt{alloc}(l, i, i')$ action represents allocating l and associating it with abstract node i, whose `link` field points to i' (which could be null). The $\texttt{upd}(i, i')$ action represents updating the `link` field of node i to point to i'. Finally, $\texttt{del}(i)$ indicates the writer's intention to deallocate node i.

Given a history H and an abstract location i, we can consider the subhistory of H containing only actions of the form $\texttt{alloc}(-, i, -)$, $\texttt{upd}(i, -)$, or $\texttt{del}(i)$. We call this the subhistory of H restricted to i, written H_i. For convenience, we treat H as a partial function, writing $H^*(i) = \top$ if $\texttt{del}(i) \in H$, and $H^*(i) = i_n \cdot \ldots \cdot i_1$ if $H_i = \texttt{alloc}(-, i, i_1) \cdot \texttt{upd}(i, i_2) \cdots \texttt{upd}(i, i_n)$. We can also consider the subtrace H_l of H containing only actions involving a physical location l. We define a similar partial function H_*, where $H_*(l) = i_n \cdot \ldots \cdot i_1$ if $H_l = \texttt{alloc}(l, i_1, -) \cdots \texttt{alloc}(l, i_n, -)$.

If the first action in H is $\texttt{alloc}(-, i, -)$, $\texttt{upd}(i, -)$, or $\texttt{del}(i)$, we say that the base of H, written $\mathsf{base}(H)$, is i. The $\mathsf{base}(H)$ is the abstract location corresponding to $q + \texttt{link}$, the pointer to the head of the list. We define $\mathsf{dead}(H)$ to be the set of all i such that $H(i) = \top$ and $\mathsf{live}(H) \triangleq \mathrm{dom}(H) \setminus \mathsf{dead}(H)$. We restrict the set of histories to "well-formed" ones, in which no node ever points to a dead node or an uninitialized node.

Histories can be ordered by saying that $H_1 \leq H_2$ if H_1 is a prefix of H_2. This ordering satisfies the following monotonicity properties, which we will use later in §6.2. If $H_1 \leq H_2$, then:

1. $\mathsf{dead}(H_1) \subseteq \mathsf{dead}(H_2)$, $\mathrm{dom}(H_1^*) \subseteq \mathrm{dom}(H_2^*)$, and $\mathrm{dom}((H_1)_*) \subseteq \mathrm{dom}((H_2)_*)$.
2. If $l \in \mathrm{dom}(H_1)$, then $(H_1)_*(l) \leq (H_2)_*(l)$, and if $i \in \mathsf{live}(H_1) \cap \mathsf{live}(H_2)$, then $H_1^*(i) \leq H_2^*(i)$.

It also satisfies the specific ordering property needed to use the master/snapshot PCM, *i.e.,* that $H_1 \leq H_3$ and $H_2 \leq H_3$ imply $H_1 \leq H_2$ or $H_2 \leq H_1$. In our RCU proof, $\Gamma.\mathsf{history}$ is an instance of this snapshot PCM. The writer is the thread that owns the authoritative Master(H), putting it in a privileged position. First of all, the thread is allowed to update the state of the history PCM to Master(H') so long as $H' \geq H$, *i.e.,* so long as the writer only *extends* the history with new actions that do not invalidate any existing snapshots. Second, the writer can copy off duplicable snapshots of this master, and then store them in the $q + \texttt{wcounter}$ counter and the `link` fields of the nodes. Since these snapshots are duplicable, they can be passed to readers as part of the protocol for Release-Acquire Pair 2. If a reader has $\boxed{\text{Snapshot}(H) : \mathsf{history}}$, then it knows that this snapshot H is a lower bound on the state of the master history. Consequently, once the reader learns that an abstract node i is in $\mathsf{dead}(H)$, it knows that the master copy can never revive i without violating dead set monotonicity, so it is safe for the reader to give up its rxtok tokens for i in Step 6 of the proof. Once an abstract node is dead, it stays dead.

"Atomic ownership" and abstract node ID histories In our explanation of the RCU proof, we described the $\mathsf{PermX}(\Gamma, l, tid, i)$ exchange as a way to transfer fractional ownership of a physical node l (with abstract ID i) back and forth between the writer and the tid-th reader. For the nonatomic `data` component of a node l, it is clear what this means: PermX serves to transfer the fractional permission $l + \texttt{data} \overset{tid}{\longhookrightarrow} v$ (along with the knowledge of the per-item invariant $P(v)$) back and forth. However, as noted at the beginning of §6, it is not clear what it means to transfer (fractional) ownership of l's *atomic* component—namely, its `link` field. Atomic locations are not (fractionally) ownable: they are governed by shared protocols and may be read/written concurrently.

Indeed, when the writer transfers "ownership" of l to reader tid, it does not actually transfer ownership of its atomic $l + \texttt{link}$ field, as this is not possible. Rather, the writer uses PermX to transfer several things which collectively suffice to enable the reader to safely access the $l + \texttt{link}$ field. First, it transfers the knowledge that $l + \texttt{link}$ obeys the **LLP** protocol (see Step 2 of the proof outline above, and more below). Second, it transfers the knowledge that the physical location l is *currently* associated with abstract ID i and that l will not be recycled and reassociated with any other abstract ID until the reader gives back its fractional ownership of the node to the writer. This is important because the reader will depend on i being a logical proxy for l in the proof; if l were to be recycled prematurely, any reasoning that the reader did based on i would not be sound.

Formally, we encode the knowledge about the association between physical locations l and abstract IDs i—along with the permission to reassociate locations with new abstract IDs when they are recycled—as elements of a second master/snapshot PCM. For each l, we keep a list of which abstract node IDs it has been associated with. The head of the list represents the node's current abstract ID. We can impose a partial ordering on these lists by saying that $L \leq L'$ if L is a suffix of L'. (This ordering satisfies the additional property needed to use the master/snapshot construction.)

When the writer first allocates a node at physical location l, it associates l with a fresh abstract node ID i by creating a new master instance j of the above PCM, initialized to store the singleton list $[i]$. Via the PermX exchange, the writer then transfers fractional ownership of j to each of its readers (*i.e.,* it gives reader tid $\boxed{j : \text{Master}_{tid}([i])}$). With this fractional ownership in hand, the readers know that the writer cannot possibly reassociate l with a different abstract ID (by advancing the state of j) because that would require it to own the full master copy of j.

Finally, the writer assigns $l + \texttt{link}$ the protocol $\mathbf{LLP}(\Gamma, l, j)$. The states of this protocol are pairs of nonempty lists $(i_0 \cdot L_0, i_1 \cdot L_1)$, where the first component represents the list of abstract IDs that l has been associated with (i_0 is the current one), and the second represents the sequence of nodes its `link` field has pointed to during the period of l's association with i_0. Note that the **LLP** protocol's interpretation of this state includes a snapshot of the PCM instance j, with state $i_0 \cdot L_0$. When the readers read $l + \texttt{link}$, this snapshot, together with their fractional ownership of j, lets them conclude that i_0 is the same abstract ID i that they know about from PermX.

During synchronization, the writer will collect all the fractional pieces of j back, so that it can safely deallocate l. The writer maintains the invariant that it owns the full master j for every node in the deallocated node pool. Hence, if the writer ends up recycling l to represent a new node, it will be able to associate a fresh abstract node ID i' with l by pushing i' onto the head of the list stored in j.

6.2 Reader Abstract Predicates

We now give the parts of the definitions of ReaderSafe and SafePtr that are relevant for accessing nodes in the list:

$$\begin{aligned}&\mathsf{ReaderSafe}(q, H, tid) \triangleq \exists \Gamma.\ \Gamma.q = q * \mathsf{SnapshotValid}(\Gamma, H)\\ &\quad * \boxed{\Gamma.\mathsf{rxtok} : \{tid\} \times (\mathbb{N} \setminus \mathsf{dead}(H))} * \text{(counter resources)}\\ &\quad * \exists j.\ \boxed{q + \texttt{link} : (\mathsf{base}(H), H^*(\mathsf{base}(H)))} \boxed{\mathbf{LLP}(\Gamma, q, j)}\\ &\qquad * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H))}\\ &\mathsf{SafePtr}(q, H, p) \triangleq \exists \Gamma.\ \Gamma.q = q * \mathsf{SnapshotValid}(\Gamma, H)\\ &\quad * (p \neq 0 \Rightarrow \exists i.\ i \notin \mathsf{dead}(H)\\ &\qquad * \forall tid < N.\ \mathsf{exch}(\mathsf{PermX}(\Gamma, p, tid, i)))\end{aligned}$$

The $\mathsf{ReaderSafe}(q, H_1, tid)$ predicate asserts that H_1 is a valid snapshot and contains all the $\Gamma.\mathsf{rxtok}$ tokens for thread tid except for the nodes that are dead in H_1. In addition, the reader is given partial "ownership" of $q + \texttt{link}$ (whose abstract node ID is fixed to be $\mathsf{base}(H_1)$ since $q + \texttt{link}$ is never deallocated). From this definition, it is clear how we lose $\mathsf{ReaderSafe}(q, H_1, tid)$ during `rcuQuiescentState`, and get back $\mathsf{ReaderSafe}(q, H_2, tid)$ for some H_2. During this function, the reader will transfer some of its $\Gamma.\mathsf{rxtok}$ into exchanges. However, it learns that $\mathsf{SnapshotValid}(H_2)$ for some new H_2, and only gives up tokens in $\mathsf{dead}(H_2)$.

$\mathsf{SafePtr}(q, H_1, p)$ just says that if p is non-null, then there exists a $\mathsf{PermX}(\Gamma, p, tid, i)$ exchange for some $i \notin \mathsf{dead}(H_1)$. By the definition of $\mathsf{ReaderSafe}(q, H_1, tid)$, the reader thus knows that it must have $\boxed{\Gamma.\mathsf{rxtok} : (tid, i)}$, so it can use this, together with the PermX exchange, to gain access to the node located at p. From this we can see why the precondition for `rcuReadNext` is sufficient.

The postcondition for `rcuReadNext` requires us to prove that when the reader does an acquire read on $p + \texttt{link}$ (line 9) and gets some value p', that $\mathsf{SafePtr}(q, H_1, p')$ is also true. Now, we know from $\mathsf{PermX}(\Gamma, p, tid, i)$ that p is associated with abstract node ID i, since the exchange contains a piece of the master PCM element listing all the abstract IDs that p has been associated with. This list has the form $i \cdot L$ for some L. Since this is part of the master copy, no other thread could have associated p with some new ID. When we read $p + \texttt{link}$, the protocol guarantees that if $p' \neq 0$, then the protocol state is of the form $(i \cdot L, i' \cdot L')$, and there exists some snapshot of an H_2 such that $H_2^*(i) = i' \cdot L'$ and $(H_2)_*(p) = i \cdot L$. In addition, we also learn that there are $\mathsf{PermX}(\Gamma, p', tid, i')$ for each tid. This gives us most of what we need in order to establish $\mathsf{SafePtr}(q, H_1, p')$—it merely remains to show that $i' \notin \mathsf{dead}(H_1)$.

Now, because of the rules for snapshot composition, either $H_1 \leq H_2$ or $H_2 \leq H_1$. In the former case, we are done, because $i' \notin \mathsf{dead}(H_2)$, and as noted in §6.1, dead sets grow monotonically. In the latter case, where $H_2 \leq H_1$, the monotonicity properties mentioned in §6.1 give us that that $(H_1)_*(p) \geq (H_2)_*(p) = i \cdot L$. However, by SnapshotValid, the reader has a snapshot of the abstract IDs that matches $(H_1)_*(p)$. Since this snapshot cannot be bigger than the master, we have $(H_1)_*(p) \leq i \cdot L$. Hence, we must have that $(H_1)_*(p) = i \cdot L$. In addition, from $\mathsf{SafePtr}(q, H_1, p)$, we know that $i \notin \mathsf{dead}(H_1)$ and thus that $H_1^*(i) \neq \top$. Using SnapshotValid again, this means that the reader already had a protocol assertion about $p + \texttt{link}$ that said it was at least in state $(i \cdot L, H_1^*(i))$. Therefore, we must have $(i \cdot L, H_1^*(i)) \leq (i \cdot L, i' \cdot L')$, which implies $H_1^*(i) \leq i' \cdot L'$. Using the monotonicity properties from §6.1 once more, since $H_1 \geq H_2$, we have that $H_1^*(i) \geq H_2^*(i) = i' \cdot L'$. Hence, $H_1^*(i) = i' \cdot L'$, and so $i' \notin \mathsf{dead}(H_1)$.

6.3 Extensions to the Basic RCU Implementation

The full version of RCU verified in the appendix contains two additional features:

- the writer batches together several node deallocations, and
- readers dynamically register themselves.

Supporting batched deallocation is straightforward. In the call to `rcuNodeUpdate`, the writer adds the old node to a deallocation stack. Then, when it wants to deallocate the stack, it performs `rcuSynchronize`, and gets the reader tokens for *all* nodes in the stack at once.

For dynamic registration, the RCU metadata contains an additional field, $q + \texttt{numreaders}$, which is a counter storing the number of readers. To register, a reader does a fetch-and-increment on this field to get their tid. During `rcuSynchronize`, the writer reads $q + \texttt{numreaders}$ and only examines the $q + \texttt{rcounters}$ entries for registered readers. For the proof, we have a protocol on $q + \texttt{numreaders}$ that initially contains $\mathsf{ReaderSafe}(q, H, tid)$ for all tid. During the fetch-and-increment, the reader takes out the $\mathsf{ReaderSafe}(q, H, tid)$ for the tid it gets assigned. Similarly, during `rcuSynchronize`, when the writer wants to deallocate the node currently associated with logical ID i, it takes out $\Gamma.\mathsf{rxtok}(tid, i)$ for all tids that have not yet been assigned to registered readers.

7. Related Work

Consume reads. The C11 memory model also includes *consume* reads, which are weaker than acquire reads and cheaper to implement efficiently on the Power and ARM architectures. With acquire reads, *everything* following the read is guaranteed to happen after the things preceding the matching release write. However, with consume reads, only the things that have a data dependency on the value read are guaranteed to happen after. For example, consider:

$$\begin{array}{l||l}
[x]_{\texttt{na}} := 25; & \texttt{let } p = [m]_{\texttt{cons}} \\
[y]_{\texttt{na}} := 37; & \texttt{if } (p \texttt{ != } 0)\ \{ \\
[m]_{\texttt{rel}} := x; & \quad [a]_{\texttt{na}} := [p]_{\texttt{na}}; \\
 & \quad [b]_{\texttt{na}} := [y]_{\texttt{na}}; \\
 & \}
\end{array}$$

In this example, the right thread's read through the pointer p is guaranteed to happen after the write that initialized x, because this access depends on the value from the consume read of m. In contrast, the access to y is racy, because it does not have a data dependency, only a control dependency. This ordering is sufficient for RCU if the reader does consume reads on the `link` field, because the accesses to the fields of the node will depend on the pointer it reads. In fact, supporting RCU was a primary motivation for including consume reads in the C11 standard. However, the standard may be revised because the current rules for data dependency tracking are too complicated, and most compilers treat consume reads as acquire reads [14]. Once these revisions are finalized, we believe it should be possible to extend GPS with support for consume reads through a modality that tracks dependencies.

User-space RCU. Our implementation of RCU is based on that of Desnoyers et al. [5], who describe a number of RCU implementations, of which QSBR is one that provides highly optimized performance. Our implementation differs from theirs in a few ways. First, their implementation uses memory barriers rather than C11 concurrency primitives. At present, there are no program logics for C11 that are as rich as GPS (in its support for protocols) and that also handle release/acquire fences and relaxed accesses. However, we believe that, assuming some handling of such mechanisms is developed in the way we imagine should be possible, our message-passing explanation will still suffice, without requiring us to revert to the notion of a grace period (see below). In particular, if the appropriate logic existed, we believe the following relaxations would be possible without changing the basic structure of our proof:

- All the release writes in `rcuNew` (lines 2, 3, 4), the write at line 19 in `rcuNodeUpdate`, and the write at line 13 in `rcuNodeAppend`

could be made relaxed (or even non-atomic). In fact, these are initialization writes, so no explicit release fence is needed.
- The reads at lines 7 and 9 could be made consume reads, as explained above.
- The read at line 32 could be made relaxed, provided we add an acquire fence after line 33.
- The reads at lines 16, 24, and 28 could be made relaxed (or non-atomic) because only the same thread can write to the field. Doing so should not affect the proof, as no real ownership transfer is performed.

In addition, Desnoyers et al.'s implementation of QSBR allows readers to go "offline" for extended periods by setting their counter field to 0. The writer's counter starts at 1, and when the writer performs `rcuSynchronize`, it checks that each reader's counter either matches its own or is 0. Later, the reader can go back online by copying the writer's counter value again. We left a proper treatment of this extension for future work because it requires a combination of weak-memory primitives and stronger synchronization operations (SC fences), for which no adequate verification techniques presently exist.

Other RCU verifications. Gotsman et al. [7] verify an RCU-based non-blocking stack implementation under a sequentially consistent memory model. Their RCU synchronization procedure is closer to exclusively using the offline/online feature of QSBR described above. They formalize the concept of a *grace period*, which is often used to informally explain RCU. A grace period is the length of time from when a node becomes unreachable until no readers are accessing it any longer. They show that this concept can be used to structure the proofs of related memory management techniques such as hazard pointers and epoch-based reclamation. Their proof uses a concurrent separation logic extended with temporal operators to make statements about the grace period. It would be interesting to try to add such temporal operators to a logic like GPS and see if a proof based on grace periods can be formalized in the setting of weak memory, but as we have shown, one can verify an RCU implementation even without them.

Alglave et al. [2] use a bounded model checker to examine a real implementation of RCU taken from the Linux kernel, which uses explicit hardware fences rather than the new C11 concurrency primitives. They apply their tool to a test harness running one reader and one writer concurrently, and verify (on several architectures) that the reader will not see malformed or uninitialized data. In contrast, we consider a simpler implementation of RCU, but provide a general proof of correctness against a modular Hoare-style specification.

Relaxed Separation Logic (RSL). One reason perhaps why there has been no prior work on formally verifying RCU in a weak-memory setting is that program logics for weak-memory concurrency have only begun appearing very recently. For instance, it was only in 2013 that Vafeiadis and Narayan [19] proposed RSL, the first program logic for the C11 memory model. RSL is a simpler logic than its sequel, GPS, and also less powerful: the GPS paper presents several examples that are beyond the scope of RSL. It is therefore instructive to consider whether we could have verified our RCU implementation using the simpler RSL. We cannot provide a definite answer whether this is possible or not, but we believe it is rather unlikely, given how heavily our proof relies on the rely-guarantee reasoning afforded by protocols, which is not directly supported in RSL.

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A. Language

A.1 Syntax

Val	V	::=	n
OVal	v	::=	$x \mid V$
Exp	e	::=	$v \mid v \texttt{ + } v \mid v \texttt{ == } v \mid v \texttt{ mod } v \mid \texttt{let } x = e \texttt{ in } e \mid \texttt{repeat } e \texttt{ end} \mid \texttt{fork } e$
		$\mid$	$\texttt{if } v \texttt{ then } e \texttt{ else } e \mid \texttt{alloc}(n) \mid [v]_O \mid [v]_O \texttt{ := } v \mid \texttt{CAS}(v,v,v) \mid \texttt{FAI}(v)$
OrderAnn	O	::=	$\texttt{at} \mid \texttt{na}$
EvalCtx	K	::=	$[\,] \mid \texttt{let } x = K \texttt{ in } e$
Action	α	::=	$\mathbb{S} \mid \mathbb{A}(\ell..\ell') \mid \mathbb{W}(\ell,V,O) \mid \mathbb{R}(\ell,V,O) \mid \mathbb{U}(\ell,V,V)$
ActName	a		(an infinite set)
ActMap	A	$\in$	$\mathit{ActName} \xrightarrow{\text{fin}} \mathit{Action}$
Graph	G	::=	$(A, \mathsf{sb}, \mathsf{mo}, \mathsf{rf}) \qquad \mathsf{sb}, \mathsf{mo} \subseteq \mathrm{dom}(A) \times \mathrm{dom}(A), \mathsf{rf} \in \mathrm{dom}(A) \rightharpoonup \mathrm{dom}(A)$
ThreadMap	T	$\in$	$\mathbb{N} \xrightarrow{\text{fin}} (\mathit{ActName} \times \mathit{Exp})$

Note: Formally, we use `at` as the notation for the memory ordering for both release release writes and acquire reads. However, when displaying programs in the main body of the paper, we have written `rel` and `acq` for clarity.

A.2 Semantics

Event steps $\boxed{e \xrightarrow{\alpha} e}$

$$
\begin{array}{rcll}
n \texttt{ + } m & \xrightarrow{\mathbb{S}} & k & k = n + m \\
n \texttt{ mod } m & \xrightarrow{\mathbb{S}} & k & k = n \bmod m \\
n \texttt{ == } m & \xrightarrow{\mathbb{S}} & 1 & n = m \\
n \texttt{ == } m & \xrightarrow{\mathbb{S}} & 0 & n \neq m \\
\texttt{let } x = V \texttt{ in } e & \xrightarrow{\mathbb{S}} & e[V/x] & \\
\texttt{repeat } e \texttt{ end} & \xrightarrow{\mathbb{S}} & \texttt{let } x = e \texttt{ in if } x \texttt{ then } x \texttt{ else repeat } e \texttt{ end} & \\
\texttt{if } V \texttt{ then } e_1 \texttt{ else } e_2 & \xrightarrow{\mathbb{S}} & e_1 & V \neq 0 \\
\texttt{if } V \texttt{ then } e_1 \texttt{ else } e_2 & \xrightarrow{\mathbb{S}} & e_2 & V = 0
\end{array}
$$

$$
\begin{array}{rcll}
\texttt{alloc}(n) & \xrightarrow{\mathbb{A}(\ell..\ell+n-1)} & \ell & \\
[\ell]_O & \xrightarrow{\mathbb{R}(\ell,V,O)} & V & \\
[\ell]_O \texttt{ := } V & \xrightarrow{\mathbb{W}(\ell,V,O)} & 0 & \\
\texttt{CAS}(\ell, V_o, V_n) & \xrightarrow{\mathbb{U}(\ell,V_o,V_n)} & 1 & \\
\texttt{CAS}(\ell, V_o, V_n) & \xrightarrow{\mathbb{R}(\ell,V',\texttt{at})} & 0 & V' \neq V_o \\
\texttt{FAI}(\ell) & \xrightarrow{\mathbb{U}(\ell,V,V')} & V & V' = (V+1) \bmod \mathbf{C} \\
K[e] & \xrightarrow{\alpha} & K[e'] & e \xrightarrow{\alpha} e'
\end{array}
$$

Machine steps $\boxed{\langle T; G\rangle \longrightarrow \langle T'; G'\rangle}$

$$
\frac{G'.A = G.A \uplus [a' \mapsto \alpha] \qquad G'.\mathsf{sb} = G.\mathsf{sb} \uplus (a, a') \qquad e \xrightarrow{\alpha} e' \qquad \mathsf{consistentC11}(G') \qquad G'.\mathsf{mo} \supseteq G.\mathsf{mo} \qquad G'.\mathsf{rf} \in \{G.\mathsf{rf},\ G.\mathsf{rf} \uplus [a' \mapsto b]\}}{\langle T \uplus [i \mapsto (a, e)]; G\rangle \longrightarrow \langle T \uplus [i \mapsto (a', e')]; G'\rangle}
$$

$$
\langle T \uplus [i \mapsto (a, K[\texttt{fork } e])]; G\rangle \longrightarrow \langle T \uplus [i \mapsto (a, K[0])] \uplus [j \mapsto (a, e)]; G\rangle
$$

The validity of these operational rules relative to the C11 standard can be found in the appendix of [17].

$$
\begin{array}{rcl}
\mathsf{execs}(e) & \triangleq & \{\ (e', G)\ \mid\ \langle [i \mapsto (\mathsf{start}, e)]; ([\mathsf{start} \mapsto \mathbb{S}], \emptyset, \emptyset, \emptyset)\rangle \longrightarrow^* \langle [i \mapsto (\_, e')] \uplus T; G\rangle\ \} \\
[\![e]\!] & \triangleq & \begin{cases} \mathbf{err} & \exists (\_, G) \in \mathsf{execs}(e).\ \mathsf{dataRace}(G) \vee \mathsf{memoryError}(G) \\ \{\ V\ \mid\ (V, \_) \in \mathsf{execs}(e)\ \} & \text{otherwise} \end{cases}
\end{array}
$$

A.3 Memory model

A.3.1 The C11 atomic access modes

The C11 standard [8] includes several kinds of atomic accesses: sequentially-consistent, release-acquire, release-consume, and fully relaxed. We have focused on release-acquire, because:

- Sequentially-consistent accesses are already well-understood.

- Release-consume atomics are useful only for specific architectures (PowerPC and Arm), but substantially complicate the memory model.
- Fully relaxed accesses, as formalized by Batty et al. [3], suffer from several known problems. First, they allow *out-of-thin-air* reads, which the text of the standard explicitly forbids [8]—but it is not known how to rule out these reads without also obstructing key compiler optimizations. On the other hand, even as formalized, fully relaxed access do not permit certain basic optimizations and pose severe problems for compositional reasoning [19, 20].

A.3.2 The formal C11 model

The C11 memory model we use is based on the formalization of Batty et al. [3], simplified in the absence of release-consume atomics. We also incorporate the following simplifications introduced by Vafeiadis and Narayan [19]:

- The sb and sw orders are not transitive; *e.g.,* sb relates each event only to its immediate successors in program order. This simplifies both the operational semantics of the language and the semantics of GPS. Since hb *is* transitively closed, this has no effect on the memory model axioms.
- The "additional synchronized with" edges are incorporated into sb rather than sw, which again makes no difference for the axioms but simplifies the semantics.
- For uniformity, the sw edges include sb-related events, whereas in [3] these are ruled out. Since hb includes both sw and sb, this makes no difference to the axioms.

In addition to these simplifications, our formalization of the memory model drops release sequences, instead requiring sw edges only between immediate atomic read/write pairs. Consequently, our axioms are strictly *weaker* than those in *e.g.,* Batty et al. [3], since we require strictly fewer sw edges. GPS does not have proof rules that take advantage of release sequences, so it is sound with or without them.

A.3.3 Axioms

$\mathsf{consistentC11}(A, \mathsf{sb}, \mathsf{mo}, \mathsf{rf}) \triangleq$

$\forall a, b.\ \mathsf{mo}(a,b) \implies \exists \ell.\ \mathsf{writes}(a,\ell,-),\ \mathsf{writes}(b,\ell,-)$ (ConsistentMO1)

$\forall \ell.\ \mathsf{strictTotalOrder}(\{a \mid \mathsf{writes}(a,\ell,-)\}, \mathsf{mo})$ (ConsistentMO2)

$\forall b.\ \ \mathsf{rf}(b) \neq \bot \iff \exists \ell, a.\ \mathsf{writes}(a,\ell,-),\ \mathsf{reads}(b,\ell,-),\ \mathsf{hb}(a,b)$ (ConsistentRF1)

$\forall a, b.\ \mathsf{rf}(b) = a \implies \exists \ell, V.\ \mathsf{writes}(a,\ell,V),\ \mathsf{reads}(b,\ell,V),\ \neg\mathsf{hb}(b,a)$ (ConsistentRF2)

$\forall a, b.\ \mathsf{rf}(b) = a, (\mathsf{isNonatomic}(a) \vee \mathsf{isNonatomic}(b)) \implies \mathsf{hb}(a,b)$ (ConsistentRFNA)

$\forall a, b.\ \mathsf{hb}(a,b) \implies$
$\quad a \neq b,\ \ \neg\mathsf{mo}(\mathsf{rf}(b), \mathsf{rf}(a)),\ \ \neg\mathsf{mo}(\mathsf{rf}(b), a),\ \ \neg\mathsf{mo}(b, \mathsf{rf}(a)),\ \ \neg\mathsf{mo}(b,a)$ (Coherence)

$\forall a, c.\ \mathsf{isUpd}(c),\ \mathsf{rf}(c) = a \implies \mathsf{mo}(a,c),\ \nexists b.\ \mathsf{mo}(a,b),\ \mathsf{mo}(b,c)$ (AtomicCAS)

$\forall a \neq b, \vec{\ell}, \vec{\ell'}.\ A(a) = \mathbb{A}(\vec{\ell}),\ A(b) = \mathbb{A}(\vec{\ell'}) \implies \vec{\ell} \pitchfork \vec{\ell'}$ (ConsistentAlloc)

where $\mathsf{hb} \triangleq (\mathsf{sb} \cup \mathsf{sw})^+$

$\mathsf{sw} \triangleq \{(a,b) \mid \mathsf{rf}(a) = b,\ \mathsf{isAtomic}(a),\ \mathsf{isAtomic}(b)\}$

$\mathsf{reads}(a,\ell,V) \triangleq A(a) \in \{\mathbb{R}(\ell,V,-), \mathbb{U}(\ell,V,-)\}$

$\mathsf{writes}(a,\ell,V) \triangleq A(a) \in \{\mathbb{W}(\ell,V,-), \mathbb{U}(\ell,-,V)\}$

$\mathsf{strictTotalOrder}(S,R) \triangleq (\nexists a.\ R(a,a)),$
$\quad (\forall a,b,c.\ R(a,b), R(b,c) \implies R(a,c)),$
$\quad (\forall a, b \in S.\ a \neq b \implies R(a,b) \vee R(b,a))$

$\mathsf{dataRace}(A, \mathsf{sb}, \mathsf{mo}, \mathsf{rf}) \triangleq \exists \ell.\ \exists a \neq b \in \mathrm{dom}(A).$
$\mathsf{accessesLoc}(a,\ell), \mathsf{accessesLoc}(b,\ell), \mathsf{writes}(a,-,-) \vee \mathsf{writes}(b,-,-),$
$\mathsf{isNonatomic}(a) \vee \mathsf{isNonatomic}(b), \neg\mathsf{hb}(a,b), \neg\mathsf{hb}(b,a)$
where $\mathsf{hb} \triangleq (\mathsf{sb} \cup \mathsf{sw})^+$

$\mathsf{memoryError}(A, \mathsf{sb}, \mathsf{mo}, \mathsf{rf}) \triangleq \exists \ell.\ \exists b \in \mathrm{dom}(A).$
$\mathsf{accessesLoc}(b,\ell),$
$\nexists a \in \mathrm{dom}(A).\ A(a) = \mathbb{A}(\vec{\ell}),\ \ \ell \in \vec{\ell},\ \ \mathsf{hb}(a,b)$
where $\mathsf{hb} \triangleq (\mathsf{sb} \cup \mathsf{sw})^+$

B. Logic

B.1 Parameters

We assume:

- The following domains, with associated metavariables:

s	$\in$	*State*	(a set)	τ	$\in$	*ProtTy*	(a set)
σ	$\in$	*ExchangeTy*	(a set)	μ	$\in$	*PCMTy*	(a set)
k	$\in$	*Permissions*	(a set)				

- For each μ, a partial commutative monoid $[\![\mu]\!]$ with unit ε_μ, multiplication $\cdot_\mu$, and a homomorphism $|-| : [\![\mu]\!] \to [\![\mu]\!]$ such that $|m| = |m| \cdot_\mu |m|$, $|m| \leq m$ and $|m| = m$ iff $m \cdot_\mu m = m$.
- For each τ a partial order $\sqsubseteq_\tau \subseteq \mathit{State} \times \mathit{State}$.
- The following interpretation functions for protocols and exchanges

$$\mathsf{interp}(\tau) \in \mathit{State} \times \mathit{Val} \to \mathit{Prop} \qquad \mathsf{interp}(\sigma) \in \mathit{Prop} \times \mathit{Prop}$$

  where if $\mathsf{interp}(\sigma) = (\mathcal{P}, \mathcal{P}')$ then $\mathcal{P} * \mathcal{P} = \emptyset$ and $\mathcal{P}' * \mathcal{P}' = \emptyset$.
- We assume *Permissions* is a permission model with a commutative, associative partial operator $\oplus$ and a full permission $\top$.
- A syntax of states, PCM terms, and permissions, with appropriate sorting rules, as part of the term syntax given below.

B.2 Syntax

Sort	θ	::=	$\mathsf{Val} \mid \mathsf{State} \mid \mathsf{PCM}_\mu$
Var	X	::=	$\ell \mid x \mid s$
Term	t	::=	$X \mid n \mid \varepsilon_\mu \mid t \cdot_\mu t \mid \cdots$
Proposition	P	::=	$t = t \mid P \wedge P \mid P \vee P \mid P \Rightarrow P \mid \forall X : \theta.\ P \mid \exists X : \theta.\ P \mid \Box P$
		$\mid$	$P * P \mid \mathsf{uninit}(t) \mid t \overset{k}{\hookrightarrow} t \mid \boxed{t : t \mid \tau} \mid t \sqsubseteq_\tau t \mid \boxed{\boxed{t : t} \mid \mu} \mid \mathsf{exch}(\sigma)$

We write $l \hookrightarrow v$ as shorthand for $l \overset{\top}{\hookrightarrow} v$

B.3 Proof theory

B.3.1 Necessitation

$$\Box P \Rrightarrow P \qquad \Box P \Rrightarrow \Box\Box P \qquad \Box P * Q \Leftrightarrow \Box P \wedge Q \qquad t = t' \Rrightarrow \Box t = t' \qquad \boxed{t : t' \mid \tau} \Rrightarrow \Box \boxed{t : t' \mid \tau}$$

$$\frac{t \cdot_\mu t = t}{\boxed{\gamma : t \mid \mu} \Rrightarrow \Box \boxed{\gamma : t \mid \mu}} \qquad \mathsf{exch}(\sigma) \Rrightarrow \Box\mathsf{exch}(\sigma)$$

B.3.2 Separation

$$\boxed{\gamma : t \mid \mu} * \boxed{\gamma : t' \mid \mu} \Leftrightarrow \boxed{\gamma : t \cdot_\mu t' \mid \mu} \qquad \boxed{\ell : s \mid \tau} * \boxed{\ell : s' \mid \tau'} \Rrightarrow \tau = \tau' \wedge (s \sqsubseteq_\tau s' \vee s' \sqsubseteq_\tau s)$$

$$\ell \overset{k}{\hookrightarrow} v * \ell \overset{k'}{\hookrightarrow} v' \Leftrightarrow v = v' \wedge \ell \overset{k \oplus k'}{\hookrightarrow} v \qquad \ell \overset{k}{\hookrightarrow} v * \boxed{\ell : s \mid \tau} \Rrightarrow \mathsf{false} \qquad \ell \overset{k}{\hookrightarrow} v * \mathsf{uninit}(\ell) \Rrightarrow \mathsf{false}$$

$$\boxed{\ell : s \mid \tau} * \mathsf{uninit}(\ell) \Rrightarrow \mathsf{false} \qquad \mathsf{uninit}(\ell) * \mathsf{uninit}(\ell) \Rrightarrow \mathsf{false}$$

B.3.3 Ghost moves

$$\frac{P \Rrightarrow Q}{P \Rrightarrow Q} \qquad \frac{P \Rrightarrow Q}{P * R \Rrightarrow Q * R} \qquad \frac{P \Rrightarrow Q \qquad Q \Rrightarrow R}{P \Rrightarrow R} \qquad \frac{\sigma : P \leftrightsquigarrow Q}{Q \Rrightarrow \mathsf{exch}(\sigma)} \qquad \frac{\sigma : P \leftrightsquigarrow Q}{P \Rrightarrow \mathsf{exch}(\sigma)} \qquad \frac{\sigma : P \leftrightsquigarrow Q}{P * \mathsf{exch}(\sigma) \Rrightarrow Q}$$

$$\frac{\sigma : P \leftrightsquigarrow Q}{Q * \mathsf{exch}(\sigma) \Rrightarrow P} \qquad \frac{P_1 \Rrightarrow Q \qquad P_2 \Rrightarrow Q}{P_1 \vee P_2 \Rrightarrow Q} \qquad \frac{P \Rrightarrow Q}{\exists X.P \Rrightarrow Q} \qquad \mathsf{true} \Rrightarrow \exists\gamma.\, \boxed{\gamma : t \mid \mu} \qquad \frac{\forall t_F : \mathsf{PCM}_\mu.\, t_1 \#_\mu t_F \Rrightarrow t_2 \#_\mu t_F}{\boxed{\gamma : t_1 \mid \mu} \Rrightarrow \boxed{\gamma : t_2 \mid \mu}}$$

B.3.4 Hoare logic

Allocation

$$\{\mathsf{true}\}\ \mathtt{alloc}(n)\ \{x.\ x \neq 0 * \mathsf{uninit}(x) * \cdots * \mathsf{uninit}(x+n-1)\}$$

Atomics

$$\frac{\forall s' \sqsupseteq_\tau s.\ \forall z.\ \tau(s', z) * P \Rrightarrow \Box Q}{\left\{\boxed{\ell : s \mid \tau} * P\right\}\ [\ell]_{\mathtt{at}}\ \left\{z.\ \exists s'.\ \boxed{\ell : s' \mid \tau} * P * \Box Q\right\}} \qquad \{\mathsf{uninit}(\ell) * \tau(s, v)\}\ [\ell]_{\mathtt{at}} := v\ \left\{\boxed{\ell : s \mid \tau}\right\}$$

$$\frac{P \Rrightarrow \tau(s'', v) * Q \qquad \forall s' \sqsupseteq_\tau s.\ \tau(s', -) * P \Rrightarrow s'' \sqsupseteq_\tau s'}{\left\{\boxed{\ell : s \mid \tau} * P\right\}\ [\ell]_{\mathtt{at}} := v\ \left\{\boxed{\ell : s'' \mid \tau} * Q\right\}}$$

$$\frac{\begin{array}{c}\forall s' \sqsupseteq_\tau s.\ \tau(s', v_o) * P \Rrightarrow \exists s'' \sqsupseteq_\tau s'.\ \tau(s'', v_n) * Q \\ \forall s'' \sqsupseteq_\tau s.\ \forall y \neq v_o.\ \tau(s'', y) * P \Rrightarrow \Box R\end{array}}{\left\{\boxed{\ell : s \mid \tau} * P\right\}\ \mathtt{CAS}(\ell, v_o, v_n)\ \left\{z.\ \exists s''.\ \boxed{\ell : s'' \mid \tau} * ((z = 1 * Q) \vee (z = 0 * P * \Box R))\right\}}$$

$$\frac{\forall s' \sqsupseteq_\tau s.\ \forall z.\ \tau(s', z) * P \Rrightarrow \exists s'' \sqsupseteq_\tau s'.\ \tau(s'', (z+1) \bmod \mathbf{C}) * Q}{\left\{\boxed{\ell : s \mid \tau} * P\right\}\ \mathtt{FAI}(\ell)\ \left\{z.\ \exists s''.\ \boxed{\ell : s'' \mid \tau} * Q\right\}}$$

Nonatomics

$$\{\mathsf{uninit}(\ell) \vee \ell \hookrightarrow -\}\ [\ell]_{\mathtt{na}} := v\ \{\ell \hookrightarrow v\} \qquad \left\{\ell \overset{k}{\hookrightarrow} v\right\}\ [\ell]_{\mathtt{na}}\ \left\{x.\ x = v * \ell \overset{k}{\hookrightarrow} v\right\} \qquad \{\mathsf{uninit}(\ell) \vee \ell \hookrightarrow -\}\ \mathtt{free}(\ell)\ \{\mathsf{true}\}$$

Structural rules

$$\frac{P' \Rrightarrow P \qquad \{P\}\ e\ \{x.\ Q\} \qquad \forall x.\ Q \Rrightarrow Q'}{\{P'\}\ e\ \{x.\ Q'\}} \qquad \frac{\{P\}\ e\ \{x.\ Q\}}{\{P * R\}\ e\ \{x.\ Q * R\}}$$

Axioms for pure reductions

$$\begin{array}{lll}\{\mathsf{true}\} & v & \{x.\ x = v\} \\ \{\mathsf{true}\} & v + v' & \{x.\ x = v + v'\} \\ \{\mathsf{true}\} & v == v' & \{x.\ x = 1 \Leftrightarrow v = v'\}\end{array} \qquad \frac{\begin{array}{c}\{P * v \neq 0\}\ e_1\ \{x.\ Q\} \\ \{P * v = 0\}\ e_2\ \{x.\ Q\}\end{array}}{\{P\}\ \mathtt{if}\ v\ \mathtt{then}\ e_1\ \mathtt{else}\ e_2\ \{x.\ Q\}} \qquad \frac{\{P\}\ e\ \{x.\ Q\} \qquad \forall x.\ \{Q\}\ e'\ \{y.\ R\}}{\{P\}\ \mathtt{let}\ x = e\ \mathtt{in}\ e'\ \{y.\ R\}}$$

$$\frac{\{P\}\ e\ \{\mathsf{true}\}}{\{P\}\ \mathtt{fork}\ e\ \{\mathsf{true}\}} \qquad \frac{\{P\}\ e\ \{x.\ (x = 0 * P) \vee (x \neq 0 * Q)\}}{\{P\}\ \mathtt{repeat}\ e\ \mathtt{end}\ \{x.\ Q\}}$$

C. RCU

We verify a simple version of quiescent-state-based reclamation (QSBR) RCU based on the implementation described by Desnoyers *et. al.* in https://www.efficios.com/pub/rcu/urcu-supp.pdf, except we batch deallocation as in http://software.imdea.org/~gotsman/papers/recycling-esop13.pdf. We make a few simplifying assumptions:

- Counters used to store the grace period generation numbers cannot overflow.
- We will work with singly linked lists rather than doubly linked lists. Although this makes the update operation less general, it simplifies the proof without avoiding the main issues.
- There is a static limit N on the number of readers.
- Reader threads never try to update entries in the list.
- We only prove safety properties; updaters can block indefinitely while waiting for readers to indicate they are in a quiescent state, and we do not prove the absence of memory leaks.
- There is a dedicated writer thread, and if a different thread becomes a writer, that ownership transfer is done through some external locking, which we don't reason about here.

We assume there is some sequentially consistent implementation of a stack, with methods `newStack`, `push` and `pop`, which we use to batch the deallocation of nodes.

Besides the extra features we verify here, there are a few differences between the implementation here and the version presented in the body of the paper:

- We use `repeat .. until` instead of while or for loops.
- The formal language does not have tuples, so `rcuReadNext` passes its return values through parameter pointers rather than by returning a tuple, as is standard in C.
- We split `rcuSynchronize` into two pieces (`rcuSynchronize` and `rcuCollect`) because these are more natural points for giving specifications.

In an earlier draft of this paper, we treated `free` as a primitive of the language and described extensions to GPS to support deallocation. This involved splitting the $\boxed{\ell : s \mid \tau}$ assertion into two pieces: one representing the permission to read or write to ℓ, and the other representing the duplicable knowledge about the lower bound on the state of the protocol.

However, earlier work on formally specifying the C11 memory model has not fully explored the semantics of `free`. This means that attempts to axiomatize its behavior and prove that the extensions of the logic are sound may not actually correspond to the semantics intended by the standard. Since our focus is on RCU rather than the semantics of deallocation in C11, we have instead implemented a way to recycle memory reclaimed during `rcuDealloc` directly, instead of calling `free`. Similarly, since we only want to show that memory *can* be safely recycled, we do not bother to make the implementation of recycling particularly efficient. We re-use the sequential implementation of the stack mentioned above to store the addresses of previously deallocated nodes. When we need to allocate a new node, we first try to pop an address off the stack and use that. If the stack is empty, we call `alloc`().

C.1 Code

```
rcuNew() ≜
  let q = alloc(N + 5)    /* q = generation counter, ptr to hd of list, number of readers, ptr to dealloc set, free stack, reader buffer */
  [q + link]_at := 0;
  [q + wcounter]_at := 0;
  let sc = alloc(1)    /* Scratch space for counter – leaks memory */
  [sc]_na := 0;
  repeat    /* somewhat awkward because there is no for loop primitive */
    let i = [sc]_na
    [q + rcounters + i]_at := 0
    [sc]_na := i + 1;
    i + 1 == N
  end;
  [q + numreaders]_at := 0;
  [q + del]_na := newStack();
  [q + free]_na := newStack();
  q

rcuAlloc(q) ≜
  let p = pop(q + free)
  if p == 0 then alloc(2)
  else p

registerReader(q) ≜
  FAI(q + numreaders)

rcuQuiescentState(q, tid) ≜
  let t = [q + wcounter]_at
  [q + rcounters + tid]_at := t;
  0

rcuSynchronize(q) ≜
  let oldgc = [q + wcounter]_at
  let newgc = oldgc + 1
  [q + wcounter]_at := newgc;
  let n = min(FAI(q + numreaders, 0), N)    /* Fetch and increment by 0 */
  if n == 0 then 0
  else
    rcuCollect(q, n, newgc)

  rcuCollect(q, n, newgc) ≜
    let sc = alloc(1)
    [sc]_na := 0;
    repeat    let i = [sc]_na
              repeat [q + rcounters + i]_at == newgc end
              [sc]_na := i + 1;
              i + 1 == n
    end;
    0

  rcuNodeAppend(q, p, v) ≜
    let x = rcuAlloc(q)    /* node = value, child pointer */
    [x + data]_na := v;
    [x + link]_at := 0;
    [p + link]_at := x;
    x

  rcuNodeUpdate(q, x, p, v) ≜
    let c = [x + link]_at
    let x' = rcuAlloc(q)    /* node = value, child pointer */
    [x' + data]_na := v;
    [x' + link]_at := c;
    [p + link]_at := x';
    rcuDealloc(q, x);
    x'

  rcuNodeDelete(q, x, p) ≜
    let c = [x + link]_at
    [p + link]_at := c;
```

```
  rcuDealloc(q, x);

rcuReadStart(q) ≜
  [q + link]_acq

rcuReadNext(q, nextptr, retptr) ≜
    /* nextptr is a pointer to a pointer to a node (ie: node** nextptr) */
    /* returns 0 and stores value of that node in retptr if it exists */
    /* otherwise returns 1 if we're at the end of the list */
  let p = [nextptr]_na
  if p == 0 then 1
  else
    let v = [p + data]_na
    let p' = [p + link]_at
    [retptr]_na := v;
    [nextptr]_na := p';
    0

rcuDealloc(q, x)
  push(q + del, x)
  let c = choose(1, 2)    /* Non-deterministically decide whether to synchronize and perform reclamation */
  if c == 1 then 0
  else
    rcuSynchronize(q)
    repeat
      let p = pop(q + del)
      if p == 0 then 1
      else
        push(q + free, p);
        0
    end
```

C.2 Specification

We try to give a simple specification for the external methods in figure 8. We assume some fixed pure predicate $P(x)$ that we require to hold of values in the list (e.g. they're all perfect squares). The specifications will require that when values are inserted, they satisfy this predicate, and that when we lookup a value, we get out something satisfying this predicate.

This specification involves several predicates that are abstract from the perspective of the client: $\mathsf{WriterSafe}(q, L)$, $\mathsf{ReaderSafe}(q, H, tid)$, $\mathsf{SafePtr}(H, p)$, and $\mathsf{ReaderQueue}(q)$. The first of these represents the permissions owned by the writer. It indicates that for the RCU structure with metadata at q, the spine of the list consists of the pointers in the logical list L. We generate this permission when we create a new RCU instance, and the writer's methods simply modify the contents of L accordingly.

The reader's analogous permission is $\mathsf{ReaderSafe}(q, H, tid)$. This H is not a list like in the writer's predicate. Rather, H is some abstract type, and all clients can do is reason about equaltiy of members of this type. This H corresponds to some sort of bound on the version of the list that the reader can see. $\mathsf{SafePtr}(q, H, p)$ means that p is a pointer that was valid with respect to this "bound" (or it is null). The reader can always get an initial SafePtr by calling `rcuReadStart`, which simply reads $q + \texttt{link}$. As the reader inspects the list using `rcuReadNext` it must feed in a valid SafePtr, and it gets another one. However, when the reader calls `rcuQuiescentState` it gets back $\mathsf{ReaderSafe}(q, H, tid)$ for some fresh H, thus making any previous SafePtr facts unusable. This forces the reader to start again at the head of the list through $q + \texttt{link}$, and is what guarantees that the writer can safely deallocate any inaccessible nodes, since the reader is unable to try to use any old pointer to the dead node.

Finally, $\mathsf{ReaderQueue}(q)$ is a duplicable predicate that indicates that $q + \texttt{numreaders}$ is initialized and readers can try to register by calling $\texttt{registerReader}(q)$.

C.3 Proof setup

C.3.1 Monoids

Master/Snapshot Monoid We will use a particular monoid construction to track the history of the list as ghost state. This monoid will allow a writer to update the history of the list by modifying a non-duplicable "master" view of it. The monoid will also contain duplicable elements called "snapshots", which are partial, possibly stale, histories of the object. Readers will use knowledge about these snapshots to reason about how the state of the list can evolve over time.

$\{\mathsf{true}\}$
  `rcuNew`()
$\{q.\, H.\, \mathsf{WriterSafe}(q, (q, \mathsf{null}) \cdot \mathtt{nil}) * \square(\mathsf{ReaderQueue}(q))\}$

$\{\mathsf{ReaderQueue}(q)\}$
  `registerReader`(q)
$\{x.\, \exists H.\, (x < N * \mathsf{ReaderSafe}(q, H, x)) \vee (x \geq N)\}$

$\{\mathsf{ReaderSafe}(q, -, tid)\}$
  `rcuQuiescentState`(q, tid)
$\{\exists H'.\, \mathsf{ReaderSafe}(q, H', tid)\}$

$\{\mathsf{ReaderSafe}(q, H, tid)\}$
  `rcuReadStart`(q)
$\{p.\, \mathsf{ReaderSafe}(q, H, tid) * \square\mathsf{SafePtr}(q, H, p)\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L')\}$
  $[p + \mathtt{link}]_{\mathsf{acq}}$
$\left\{\begin{array}{l} p'.\, \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L') * ((p' = 0 \wedge L' = \mathtt{nil}) \\ \quad \vee (p' \neq 0 \wedge \exists L'', v'.\, L' = (p', v') \cdot L'')) \end{array}\right\}$

$\{\mathsf{ReaderSafe}(q, H, tid) * nextptr \hookrightarrow p * \mathsf{SafePtr}(q, H, p) * retptr \hookrightarrow -\}$
  `rcuReadNext`$(q, nextptr, retptr)$
$\{x.\, \exists v, p'.\, \mathsf{ReaderSafe}(q, H, tid) * nextptr \hookrightarrow p' * \square(\mathsf{SafePtr}(q, H, p')) * retptr \hookrightarrow v * ((x = 0 \wedge P(v)) \vee x = 1)\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v)) * \square P(v')\}$
  `rcuNodeAppend`(q, p, v')
$\{x.\, \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot (x, v'))\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L') * \square P(v_1')\}$
  `rcuNodeUpdate`(q, x, p, v_1')
$\{x'.\, \mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x', v_1') \cdot L')\}$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L')\}$
  `rcuNodeDelete`(q, x, p)
$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot L')\}$

Figure 8. Full specifications for client API

Suppose P is a partially ordered set with a bottom element and the additional property[2] that for all $x, y, z \in P$, if $x \leq z$ and $y \leq z$ then either $x \leq y$ or $y \leq x$. We can now define a PCM μ_P which has elements of the form $\text{Master}_k(p)$ and $\text{Snapshot}(p)$ for each $p \in P$ and $k \in \mathit{Permissions}$. Then $\cdot$ is defined by:

$$\text{Master}_k(p) \cdot \text{Master}_{k'}(p') \triangleq \text{Master}_{k''}(p) \text{ iff } p = p' \text{ and } k \oplus k' = k''$$
$$\text{Snapshot}(p) \cdot \text{Master}_k(p') \triangleq \text{Master}_k(p') \text{ iff } p \leq p'$$
$$\text{Master}_k(p) \cdot \text{Snapshot}(p') \triangleq \text{Master}_k(p) \text{ iff } p' \leq p$$
$$\text{Snapshot}(p) \cdot \text{Snapshot}(p') \triangleq \text{Snapshot}(\max(p, p')) \text{ if this exists}$$

We will write $\text{Master}(p)$ as an abbreviation for $\text{Master}_\top(p)$. If $p \leq p'$ then we can ghost update an instance of $\text{Master}(p)$ to $\text{Master}(p')$ since the only things compatible with $\text{Master}(p)$ are elements of the form $\text{Snapshot}(p'')$ such that $p'' \leq p$, and these will also be compatible with $\text{Master}(p')$. We will instantiate this definition for two different posets in the proof. The first, will be over the poset of *traces*, which is described in the next section. The second will be with lists of natural numbers, under the ordering where $l_1 \leq l_2$ if l_1 is a suffix of l_2. Since these two posets are disjoint, it should be clear from context which instance of the monoid we are considering.

Traces We construct a partially ordered set of traces describing the history of the linked list. This partially ordered set has the additional property needed for the master/snapshot monoid.

Traces will be lists of abstract *actions*, where actions are of the form: $\mathtt{alloc}(l, i, i')$, $\mathtt{upd}(i, i')$ or $\mathtt{del}(i)$ where $l, i \in \mathbb{N}$ and $i' \in \mathbb{N} \cup \{\mathsf{null}\}$. The first represents associating a physical node located at l with some *abstract node* i, which points to i'. The second represents updating the link pointer for the physical node associated with abstract node i to point to the physical location associated with node i' (if $i' \in \mathbb{N}$) or null (if $i' = \mathsf{null}$). The final action indicates deallocating an abstract node (which means that the associated physical location will become a candidate for being associated with a new abstract node). Given a trace H and an abstract location i, we can consider the subtrace of H containing

[2] Alternatively, we can say that every principal ideal of P is totally ordered.

only actions of the form $\texttt{alloc}(()-, i, -)$, $\texttt{upd}(i, -)$ or $\texttt{del}(i)$. We call this the subtrace of H restricted to i, written H_i. We can similarly consider the subtrace of H containg only actions of the form $\texttt{alloc}(l, -, -)$ for some l. We call this $H_{|l}$ to indicate this subtrace. If the first action in H is either $\texttt{alloc}(-, i, -)$, $\texttt{upd}(i, -)$ or $\texttt{del}(i)$ we say that the base of H, written $\mathsf{base}(H)$, is i. The $\mathsf{base}(H)$ will be the abstract location corresponding to $q + \texttt{link}$.

We say that a trace is in a valid configuration if:

1. For all i, if H_i is non-empty, then the first entry is of the form $\texttt{alloc}(l, i, i')$ for some l and i', and no other instance of $\texttt{alloc}()$ occurs in H_i.
2. For all i, if $\texttt{del}(i) \in H$, it occurs at most once, and is the last action of H_i.
3. $\nexists i, j, L_i, L_j$ such that $(H_i = L_i \cdot \cdots \texttt{del}(i) \vee H_i = \texttt{nil})$ and $(H_j = L_j \cdot \texttt{upd}(j, i) \vee H_j = L_j \cdot \texttt{alloc}(-, j, i))$.

Together, these mean that no node currently points to a dead node or an uninitialized node, and we haven't tried to update the pointer of a dead node or delete it twice, we don't try to allocate an abstract node twice, and we don't associate a physical location with two abstract nodes without deallocating one of them first. We say that H is well-formed if H and all of its prefixes are in valid configurations. From here onward, we restrict our attention to well-formed traces.

Given a trace H, we can define a partial function H^* with a finite domain from $\mathbb{N}$ to $(\mathit{List}\ (\mathbb{N} \cup \{\mathsf{null}\}) \cup \{\top\}$ as follows:

$$H^*(i) = \begin{cases} \top & \text{if } \texttt{del}(i) \in H \\ i_n \cdot \ldots \cdot i_1 \cdot \texttt{nil} & \text{if } H_i = \texttt{alloc}(-, i, i_1) \cdots \texttt{upd}(i, i_n) \qquad \text{(so } H_i \text{ must be non-empty)} \end{cases}$$

This function maps an abstract node in the domain to the sequence of abstract nodes it has pointed to. The order of $H^*(i)$ is opposite the order that the updates occurred, so that the head of the list is the most recent thing to which i points. We will often just drop the * and simply write $H(i)$.

We can also define a similar partial function mapping physical locations to the abstract nodes they've been associated with. We write this partial function as H_*:

$$H_*(l) = \left\{ i_n \cdot \ldots \cdot i_1 \cdot \texttt{nil} \quad \text{if } H_{|l} = \texttt{alloc}(l, i_1, -) \cdot \texttt{alloc}(l, i_2, -) \cdots \texttt{alloc}(l, i_n, -) \right.$$

We will always write $H_*(l)$ instead of just $H(l)$ to avoid ambiguity with H^*. We write $H^*_*(l)$ as shorthand for $H^*(\mathsf{hd}(H_*(l)))$.

We order traces by saying that $H_1 \leq H_2$ if H_1 is a prefix of H_2. This is a partial order with the property that if $H_1 \leq H_3$ and $H_2 \leq H_3$ then $H_1 \leq H_2$ or $H_2 \leq H_1$. Note that if $H_1 \leq H_2$ then $\mathrm{dom}(H_1^*) \subseteq \mathrm{dom}(H_2^*)$ and $\forall i \in \mathrm{dom}(H_1^*).\ H_1^*(i) \leq H_2^*(i)$ where we order $(\mathit{List}\ (\mathbb{N} \cup \{\mathsf{null}\}) \cup \{\top\}$ by:

$$L \leq \top \qquad\qquad L_1 \leq L_2 \Leftrightarrow \exists L'.\ L_2 = L' \cdot L_1$$

The H_* is monotonic in a similar manner.

We define $\mathsf{dead}(H)$ and $\mathsf{live}(H)$ as the finite sets:

$$\mathsf{dead}(H) \triangleq \{i \mid H(i) = \top\}$$
$$\mathsf{live}(H) \triangleq \mathrm{dom}(H) \setminus \mathsf{dead}(H)$$

We have the properties that $\mathsf{live}(H) \cap \mathsf{dead}(H) = \emptyset$ and if $H \leq H'$, then $\mathsf{dead}(H) \subseteq \mathsf{dead}(H')$. Hence if $H \leq H'$, then $\mathsf{dead}(H) \cap \mathsf{live}(H') = \emptyset$.

Notice that the restrictions we've placed on traces do not rule out cycles. In particular, a single node may be pointed to by two others, or itself. We have a separate predicate that captures this:

$$\mathsf{SinglePtr}(H) \triangleq (\forall i, i'.\ \mathsf{hd}(H(i)) = \mathsf{hd}(H(i')) \Rightarrow i = i') \wedge (\forall i.\ \mathsf{hd}(H(i)) \neq i) * (\forall i.\ \mathsf{hd}(H(i)) \neq \mathsf{base}(H))$$

The final conjunct here states that no node loops back to the metadata for the RCU instance, since $\mathsf{base}(H)$ corresponds to $q + \texttt{link}$. This definition still allows abstract cycles of the form $i \to j \to \cdots \to k \to i$, but these cycles must not be connected to the real list whose head is pointed to by $q + \texttt{link}$, since we know that i cannot be $\mathsf{base}(H)$ and no node other than k can point to i, and $\mathsf{base}(H)$ cannot occur in the above cycle.

Monoid Instances Since we will work with a number of monoid instances, to simplify things we will use Γ as a metavariable for a record containing all of the relevant monoid instances. $\Gamma.\mathsf{history}$ will refer to the instance of the master/snapshot monoid with traces as the poset. We also use the powerset of $\{0, \ldots, N\} \times \mathbb{N}$ monoid with disjoint union as composition. We will work with three instances of this monoid: $\Gamma.\mathsf{rxtok}$, which represents the tokens used by threads to access elements of the linked list, $\Gamma.\mathsf{wxtok}$, which is for the tokens that the writer will use to retrieve these access tokens when it needs to deallocate a node, and $\Gamma.\mathsf{ctok}$ which are tokens used by the threads to update their version counter. The $\{0, \ldots, N-1\} \times \mathbb{N}$ of the access tokens and counter tokens are used by readers, while $\{N\} \times \mathbb{N}$ is reserved for the writer. Lastly, $\Gamma.q$ will correspond to the physical location that the RCU meta-data is located at.

Note that other monoid instances will appear. They are used in the way we link physical locations to the abstract locations mentioned in the traces. However, we do not bother to name them because they do not appear in the specifications for many protocols.

C.3.2 Protocols and Exchanges

Release-Acquire Pair 1 We will need to split permissions to access the nodes into partial pieces for readers (and one for the writer to retain). Our permissions will be subsets of $\{0, \ldots, N\}$ where $\top$ is the full set, and composition is defined as $\uplus$. We will often write the singleton permission $\{n\}$ as n.

First, to transmit ownership of the nodes, we have a family of exchanges, $\mathsf{PermX}(\Gamma, l, tid, i)$ of the form:

$$\mathsf{PermX}(\Gamma, l, tid, i) \triangleq \boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}} \rightsquigarrow \left((\exists v.\, l + \mathtt{data} \xhookrightarrow{tid} v * P(v)) * (\exists j, L. \boxed{l + \mathtt{link} : (i \cdot L, -) \mid \mathbf{LLP}(\Gamma, l, j)} * \boxed{j : \mathrm{Master}_{tid}(i \cdot L)}\right)$$

The left side of this exchange is reader tid's ith access token. The right side contains two pieces. First, there is the fractional permission to read the $l + \mathtt{data}$ field, as well as the knowledge that the value stored in that field satisfies the predicate P. The second part is the knowledge that the $l + \mathtt{link}$ field is an atomic location at least in some state on the protocol **LLP** (defined below), as well as a fractional piece of some master copy of ghost state. While the protocol assertion provides a lower bound on the state of $l + \mathtt{link}$, the ghost state acts as an upper bound on this state, as we shall see below.

As indicated above, we use a family of protocols of the form $\mathbf{LLP}(\Gamma, j)$ where $j \in \mathbb{N}$ for the `link` fields of the nodes. The states of this protocol are pairs whose first components are non-empty lists of natural numbers and whose second components are non-empty elements of $List\ (\mathbb{N} \cup \{\mathsf{null}\})$. The ordering is lexicographic, where the ordering on the lists is $l \leq l'$ iff $\exists l''.\, l' = l'' \cdot l$. The protocol interpretation is:

$$\begin{aligned}
\mathbf{LLP}(\Gamma, l, j)((i \cdot L_0, \mathsf{null} \cdot L_1), x) \triangleq\ & x = 0 * \boxed{j : \mathrm{Snapshot}(i \cdot L_0)} * \exists H. \boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H)} * H(i) = \mathsf{null} \cdot L_1 \\
& * H_*(l) = i \cdot L_0 \\
\mathbf{LLP}(\Gamma, l, j)((i \cdot L_0, i' \cdot L_1), x) \triangleq\ & x \neq 0 * \boxed{j : \mathrm{Snapshot}(i \cdot L_0)} * \exists H. \boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H)} * H(i) = i' \cdot L_1 \\
& * H_*(l) = i \cdot L_0 * H_*(x) = i' \cdot - * (\forall tid < N. \mathsf{PermX}(\Gamma, x, tid, i'))
\end{aligned}$$

The first component of these states represents the list of abstract nodes that the physical location l has been associated with. The second component is the list of abstract nodes which have been l's child (the list also includes null to represent moments when l had no children). The interpretation is composed of several pieces:

1. If l currently has no child, (i.e. the head of the second component of the state is null), then x, the value currently stored in $l + \mathtt{link}$ must be 0, but otherwise it should be non-zero.
2. Next, there is an element of the j monoid instance, which is supposed to be a snapshot matching the first component of the state. Previously, we mentioned how the fractional master state in the PermX exchange acted as an upper bound on the protocol state of $l + \mathtt{link}$. This piece of ghost state in the interpretation is what guarantees that. Suppose the a reader thread owns $\boxed{j : \mathrm{Master}_{tid}(i \cdot L)}$ and knows $\boxed{l + \mathtt{link} : i \cdot L, - \mid \mathbf{LLP}(\Gamma, j)}$. Then, when it does an acquire read of $l + \mathtt{link}$ and learns that it is in some state $(i' \cdot L', L'')$, it will be able to prove that $i' \cdot L' = i \cdot L$. By the protocol assertion we know that $i \cdot L \leq i' \cdot L'$. In addition, the interpretation would contain $\boxed{j : \mathrm{Snapshot}(i' \cdot L')}$, but we know that $\mathrm{Master}_{tid}(i \cdot L) \cdot \mathrm{Snapshot}(i' \cdot L')$ must be defined, which guarantees that $i' \cdot L' \leq i \cdot L$. Thus we have that $i \cdot L = i' \cdot L'$.
3. There is a snapshot of some trace which in which l really points to the abstract node i, which in turns points to either i' or null, so that it matches the head of the second component of the protocol state. The importance of this piece is explained later on.
4. If l does in fact have a child, then there is knowledge that a PermX exchange exists for the permissions to access the child's fields.

Release-Acquire Pair 2 Recall that as part of this release-acquire pair, the writer will request permission to deallocate some set of nodes. To do so, it needs to indicate to the readers that it has made some set of nodes unreachable. To do this, it stores a snapshot in which these nodes are inaccessible. However, it also needs to assert that the physical state of the list actually corresponds to the representation in the snapshot. We define a predicate $\mathsf{SnapshotValid}(\Gamma, H)$ which connects a snapshot to its implied interpretation about the state of `link` fields:

$$\begin{aligned}
\mathsf{SnapshotValid}(\Gamma, H) \triangleq\ & H \neq \mathtt{nil} * \boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H)} * \mathsf{base}(H) \notin \mathsf{dead}(H) * H_*(\Gamma.q) = \mathsf{base}(H) \cdot \mathtt{nil} \\
& * (\forall l \in \mathrm{dom}(H_*).\ \exists j. \boxed{j : \mathrm{Snapshot}(H_*(l))} * \boxed{l + \mathtt{link} : - \mid \mathbf{LLP}(\Gamma, l, j)} \\
& * H^*(\mathsf{hd}(H_*(l))) \neq \top \Rightarrow \boxed{l + \mathtt{link} : H_*(l), H^*_*(l) \mid \mathbf{LLP}(\Gamma, l, j)})
\end{aligned}$$

The protocol $\mathbf{WCP}(\Gamma)$ will be used for the writer's generation counter. The states of the protocol will be elements of $Traces \times \mathbb{N}$ ordered such that:

$$(H, v) \leq (H', v') \qquad \text{iff} \qquad (H = H' \wedge v \leq v') \vee (H \leq H' \wedge v < v')$$

The interpretation is:

$$\mathbf{WCP}(\Gamma)((H, v), x) \triangleq x = v * \boxed{\Gamma.\mathsf{ctok} : \{(N, v)\}} * \mathsf{SnapshotValid}(\Gamma, H)$$

The ghost state tokens here are just to enforce the fact that only the writer thread is allowed to write to this location.

Release-Acquire Pair 3 To transfer the rxtok to the writer as part of this release-acquire pair, we have a family of exchanges of the form $\mathsf{ModX}(\Gamma, tid, i)$:

$$\mathsf{ModX}(\Gamma, tid, i) \triangleq \boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}} \rightsquigarrow \boxed{\Gamma.\mathsf{wxtok} : \{(tid, i)\}}$$

We then have a protocol assertion for the generation counters for the readers, $\mathbf{RCP}(\Gamma, tid)$ which has the same states and ordering as **WCP**. The protocol interpretation is:

$$\begin{aligned}
\mathbf{RCP}(\Gamma, tid)((H, v), x) \triangleq\ & x = v * \boxed{\Gamma.q + \mathtt{wcounter} : (H, v) \mid \mathbf{WCP}(\Gamma)} * \boxed{\Gamma.\mathsf{ctok} : \{(tid, v)\}} \\
& * (\forall i \in \mathsf{dead}(H).\ \mathsf{ModX}(\Gamma, tid, i))
\end{aligned}$$

Registering Readers We have a protocol $\mathbf{NRP}(\Gamma)$ on $\Gamma.q + \texttt{numreaders}$. The states of the protocol are the same as those of **WCP** and **RCP**, but this time ordered pointwise. Initially, this protocol stores all of the ReaderSafe permissions (defined below) for each possible reader thread. As readers register, they take out the permissions corresponding to the reader ID they're assigned. Similarly, when the writer wants to deallocate a node, it takes out the permissions from that node for the threads that haven't yet registered.

$$\mathbf{NRP}(\Gamma)((H, v), x) \triangleq x = v * \left(\mathop{\Large *}_{v \leq tid < N} \mathsf{ReaderSafe}(\Gamma.q, H, tid) \right)$$

Abstract Predicates for Reader Invariants The idea is that a reader maintains the invariant that they have knowledge of some H such that $\mathsf{SnapshotValid}(\Gamma, H)$, and $\forall i \in \mathbb{N}$ either the reader owns $\boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}}$ or $i \in \mathsf{dead}(H)$. In general, every time a reader reads $l + \texttt{link}$ field of node it encounters from this point on, it will be in a situation where it will know $\boxed{l + \texttt{link} : (i_1 \cdot L_1, i_2 \cdot L_2) \mid \mathbf{LLP}(\Gamma, l, j)}$ for some i_1, L_1, i_2, L_2, and j, where one of the following three is true:

1. l is not in the domain of H,
2. $H_*(l) < i_1 \cdot L_2$, or
3. $(H_*(l) = i_1 \cdot L_1 \wedge H^*(i_1) \leq i_2 \cdot L_2)$

Furthermore, it will have $\boxed{j : \mathrm{Master}_{tid}(i_1 \cdot L_1)}$ We show that this is sufficient to guarantee that reader will be able to acccess the data field of the child it learns about by reading $l + \texttt{link}$, and that it will be able to establish the above properties for the child's $\texttt{link}$ field.

Initially, the above properties for the $q + \texttt{link}$ field are guaranteed by the AccessList predicate that the reader will own. For the inductive case[3], assume that $l + \texttt{link}$ satisfies the above. Then we will show that when the readers reads some value l' from this field, then if $l' \neq 0$, then $l' + \texttt{link}$ will satisfy the above. When the reader reads $l + \texttt{link}$, it will learn that the new state of $l + \texttt{link}$ must be of the form $(i_1 \cdot L_1, i_2' \cdot L_2')$ for some $i_2' \cdot L_2'$ where $i_2 \cdot L_2 \leq i_2' \cdot L_2'$, and it gets ownership of some $\mathrm{Snapshot}(H')$ where $H'_*(l) = i_1 \cdot L_2$ and $H'(i_1) = i_2' \cdot L_2'$. (Recall from above that we showed why the first component cannot change.) Since $\mathrm{Snapshot}(H) \cdot \mathrm{Snapshot}(H')$ must be defined, either $H \leq H'$ or $H' \leq H$. Consider the two cases:

- $H \leq H'$: Then $i_2' \in \mathsf{live}(H')$ (or else H' would not be well-formed), so $i_2' \notin \mathsf{dead}(H)$, by the properties described above about the ordering of traces and deadsets. This means that the reader owns $\boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}}$, so it will be able to use the $\mathsf{PermX}(\Gamma, l', tid, i_2')$ exchange it learns about when it read $l + \texttt{link}$. In addition to letting it access the child's data field, this will get it knowledge that $\boxed{l' + \texttt{link} : (i_2' \cdot L_2'', -) \mid \mathbf{LLP}(\Gamma, l', j')}$ and $\boxed{j' : \mathrm{Master}_{tid}(i_2' \cdot L_2'')}$ for some j' and L_2''.

  We just need to show that we have a protocol assertion about $l' + \texttt{link}$ which satisfies one of the three conditions above. Now, either l' is already in $\mathrm{dom}(H_*)$ or not. If not, we're done, and we can use the protocol assertion from the exchange.
  If it is, then by SnapshotValid, the thread has $\boxed{j'' : H_*(l'')}$ and $\boxed{l' + \texttt{link} : (-, -) \mid \mathbf{LLP}(\Gamma, l, j'')}$ for some j''. Now, by the separation rules for protocol assertions, we must have that $j' = j''$. Then, from the composition rules for snapshot/master elements, we must have that $H_*(l') \leq i_2' \cdot L_2''$. Therefore, either $H_*(l') < i_2' \cdot L_2''$ or $H_*(l') = i_2' \cdot L_2''$. Again, in the former the protocol assertion from the exchange works and satisfies condition 2 from above. Finally if $H_*(l') = i_2' \cdot L_2''$, then since we already know $i_2' \notin \mathsf{dead}(H)$, by SnapshotValid, we already have a protocol assertion of the form $\boxed{l' + \texttt{link} : (i_2' \cdot L_2', H_*(i_2')) \mid \mathbf{LLP}(\Gamma, l', j')}$. At this point we can take the max of the protocol assertion from the exchange and this one we get from SnapshotValid, and we're done.

- $H' \leq H$: Then we can conclude that $l \in \mathrm{dom}(H_*)$ because the domains of traces grow monotonically. Moreover, this montonicity also guarantees that we must have that $H_*(l) \geq i_1 \cdot L_1$ This implies that we're in the third case above, so $H^*(i_1) \leq i_2 \cdot L_2 \leq i_2' \cdot L_2'$. But at the same time, we must have that $H^*(i_1) = i_2' \cdot L_2'$, since otherwise we would have $H^*(i_1) < H'^*(i_1)$, which is impossible if $H' \leq H$. Hence, $i_2' \in \mathsf{live}(H)$, so $i_2' \notin \mathsf{dead}(H)$. This means that the reader will be able to use the $\mathsf{PermX}(\Gamma, l', tid, i_2')$. At this point the argument for the previous case applies.

In summary, if a thread knows a particular snapshot is valid, and has all of the rxtok for some tid, then it has "permission" to access the list. We define abstract predicates that capture this and other things the reader has to maintain:

$$\begin{aligned}
\mathsf{AccessList}(\Gamma, H, tid) &\triangleq \mathsf{SnapshotValid}(\Gamma, H) * \boxed{\Gamma.\mathsf{rxtok} : \{tid\} \times (\mathbb{N} \setminus \mathsf{dead}(H))} \\
&\quad * \exists j. \boxed{\Gamma.q + \texttt{link} : (\mathsf{base}(H) \cdot \texttt{nil}, H(\mathsf{base}(H))) \mid \mathbf{LLP}(\Gamma, \Gamma.q, j))} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})} \\
\mathsf{RCounterValid}(\Gamma, H, tid) &\triangleq \exists v_1, v_2, H'. (H', v_1) \leq (H, v_2) * \boxed{\Gamma.q + \texttt{wcounter} : (H, v_2) \mid \mathbf{WCP}(\Gamma)} \\
&\quad * \boxed{\Gamma.q + \texttt{rcounters} + tid : (H', v_1) \mid \mathbf{RCP}(\Gamma, tid)} \\
&\quad * \boxed{\Gamma.\mathsf{ctok} : \{tid\} \times (\mathbb{N} \setminus \{0, \ldots, v_1\})} \\
&\quad * (\forall i \in \mathsf{dead}(H). \mathsf{ModX}(\Gamma, tid, i)) \\
\mathsf{ReaderSafe}(q, H, tid) &\triangleq \exists \Gamma. \Gamma.q = q * \mathsf{AccessList}(\Gamma, H, tid) * \mathsf{RCounterValid}(\Gamma, H, tid) \\
\mathsf{SafePtr}(q, H, p) &\triangleq \exists \Gamma. \mathsf{SnapshotValid}(\Gamma, H) * \left((p = 0) \vee (p \neq 0 * \exists i'. i' \notin \mathsf{dead}(H) * \mathsf{PermX}(\Gamma, p, tid, i'))\right) \\
\mathsf{ReaderQueue}(q) &\triangleq \exists \Gamma, H, v. \Gamma.q = q * \boxed{q + \texttt{numreaders} : (H, v) \mid \mathbf{NRP}(\Gamma)}
\end{aligned}$$

[3] We only mean inductive in an informal sense here. What we actually mean is that what will be the precondition for part of `rcuReadNext`will be strong enough to satisfy the post condition.

Abstract Predicates for Writer Invariants $\mathsf{WriterSafe}(q, L)$, the analogue of ReaderSafe for writers, is more complicated. At the top, it states that the most recent update done by the writer put the list in a state where the list contains the pointers and value fields in the abstract list L. Underneath, it states that there are three traces, H_1, H_2, and H_3 such that the last time the writer's counter was modified, the list trace was H_1, everything in the deallocation stack is in $\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1)$, the most up-to-date trace is H_3, and the writer's counter and tokens adequately reflect these facts.

$$\begin{aligned}
\mathsf{RevokedUpTo}(\Gamma, H) &\triangleq \exists v, v'.\, \boxed{q + \texttt{wcounter} : (H, v) \mid \mathbf{WCP}(\Gamma)} * \boxed{\Gamma.\mathsf{ctok} : \{N\} \times (\mathbb{N} \setminus \{0, \ldots, v\})} \\
&\quad * \boxed{q + \texttt{numreaders} : (H, v') \mid \mathbf{NRP}(\Gamma)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N\} \times (\mathbb{N} \setminus \mathsf{dead}(H))} \\
\mathsf{DeallocBetween}(\Gamma, H_1, H_2) &\triangleq \exists L_d, L_d'.\, \mathsf{Stack}(\Gamma.q + \texttt{del}, L_d) * \mathsf{NoDup}(L_d) * \mathsf{NoDup}(L_d') * \mathsf{DeadFrom}(L_d, L_d', H_1, H_2) \\
\mathsf{CurrentState}(\Gamma, L, H) &\triangleq \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H)} * \mathsf{SnapshotValid}(H) * \mathsf{TraceSpine}(\Gamma, H, L) * \mathsf{SinglePtr}(H) \\
\mathsf{FreeValid}(\Gamma) &\triangleq \exists L_f.\, \mathsf{Stack}(\Gamma.q + \texttt{free}, L_f) \\
&\quad * \left(\ast_{i<|L_f|} \exists j, S.\, \boxed{L_f[i] + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L_f[i], j)} * \boxed{j : \mathrm{Master}(S)} * L_f[i] + \texttt{data} \hookrightarrow -\right) \\
\mathsf{WriterSafe}(q, L) &\triangleq \exists \Gamma, H_1, H_2, H_3.\, \Gamma.q = q * H_1 \le H_2 \le H_3 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{FreeValid}(\Gamma) \\
&\quad * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{CurrentState}(\Gamma, L, H_3) \\
\mathsf{NoDup}(L) &\triangleq \forall i, i'.\, L[i] = L[i'] \Rightarrow i = i' \\
\mathsf{TraceSpine}(\Gamma, H, L) &\triangleq \exists L'.\, |L| = |L'| * (\forall i < |L'| - 1. L'[i] \in \mathsf{live}(H) \wedge \mathsf{hd}(H(L'[i])) = L'[i+1]) \\
&\quad * \left(\ast_{1 \le i < |L|} (\pi_1\, L[i]) + \texttt{data} \overset{N}{\hookrightarrow} (\pi_2\, L[i]) * (\forall tid < N.\, \mathsf{PermX}(\Gamma, (\pi_1\, L[i]), i, tid, L'[i]))\right) \\
&\quad * L[0] = (\Gamma.q, \mathsf{null}) * \mathsf{hd}(H(L'[|L'| - 1])) = \mathsf{null} \\
&\quad * \left(\ast_{i<|L|} \exists j, R.\, \boxed{(\pi_1\, L[i]) + \texttt{link} : ((L'[i] \cdot R), H(L'[i])) \mid \mathbf{LLP}(\Gamma, \pi_1\, L[i], j)}\right. \\
&\qquad \left. * \boxed{j : \mathrm{Master}_N(L'[i] \cdot L)}\right) \\
\mathsf{DeadFrom}(\Gamma, L_d, L_d', H_1, H_2) &\triangleq |L_d| = |L_d'| * \left(\ast_{j<|L_d|} L_d'[j] \in \mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1) * (\forall n < N.\, \mathsf{PermX}(\Gamma, L_d[j], n, L_d'[j]))\right. \\
&\qquad \left. L_d[j] + \texttt{data} \overset{N}{\hookrightarrow} - * \exists j', S.\, \boxed{L_d[j] + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L_d[j], j')} * \boxed{j : \mathrm{Master}_N(S)}\right)
\end{aligned}$$

C.4 Hoare proofs

C.4.1 Verification of `rcuNew`

The specification for `rcuNew` says that at the end we get all of the permissions that the writer thread needs. From there, we could transfer these to some other writer, and transmit knowledge of the $q + \texttt{numreaders}$ counter to readers through whatever means we like.

$\{\mathsf{true}\}$
`rcuNew()`
$\{q.\, \mathsf{WriterSafe}(q, [(q, \mathsf{null})]) * \mathsf{ReaderQueue}(q)\}$

For concision, we use the following abstract predicate in this proof:

$$\begin{aligned}
\mathsf{RCountersInitUpTo}(\Gamma, \varphi, j, S) &\triangleq \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(\mathrm{upd}(\varphi, \mathsf{null}))} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times \mathbb{N}} \\
&\quad * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N\} \times \mathbb{N}} * \boxed{\Gamma.\mathsf{ctok} : \{0, \ldots, j-1\} \times (\mathbb{N} \setminus \{0\})} \\
&\quad * \boxed{\Gamma.\mathsf{ctok} : \{j, \ldots, N-1\} \times \mathbb{N}} * \boxed{\Gamma.\mathsf{ctok} : \{N\} \times (\mathbb{N} \setminus S)} \\
&\quad * \left(\ast_{tid<j} \boxed{\Gamma.q + \texttt{rcounters} + tid : (\mathsf{alloc}(\Gamma.q, \varphi, \mathsf{null}), 0) \mid \mathbf{RCP}(\Gamma)}\right) \\
&\quad * \left(\ast_{j \le tid < N} \mathsf{uninit}(\Gamma.q + \texttt{rcounters} + tid)\right)
\end{aligned}$$

$\{\mathsf{true}\}$
`let` $q = \mathsf{alloc}(N + 5)$ *`/* q = generation counter, ptr to head of list, number of readers, ptr to dealloc set, reader buffer */`*
$\{\square(q \neq 0) * \mathsf{uninit}(q + \texttt{wcounter}) * \mathsf{uninit}(q + \texttt{link}) * \mathsf{uninit}(q + \texttt{numreaders}) * \mathsf{uninit}(q + \texttt{del}) * \mathsf{uninit}(q + \texttt{free})$
$\quad * \left(\ast_{tid<N} \mathsf{uninit}(q + \texttt{rcounters} + tid)\right)\}$

$\left\{\begin{array}{l}\mathsf{uninit}(\varphi) * \mathsf{uninit}(q + \mathtt{wcounter}) * \mathsf{uninit}(q + \mathtt{link}) * \mathsf{uninit}(q + \mathtt{numreaders}) * \mathsf{uninit}(q + \mathtt{del}) * \mathsf{uninit}(q + \mathtt{free}) \\ \quad * \left(\ast_{tid<N} \mathsf{uninit}(q + \mathtt{rcounters} + tid)\right)\end{array}\right\}$

$\left\{\begin{array}{l}\exists \Gamma, j.\, \mathsf{RCountersInitUpTo}(\Gamma, 0, 0, \emptyset) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \Gamma.q = q * \mathsf{uninit}(q + \mathtt{wcounter}) * \mathsf{uninit}(q + \mathtt{link}) \\ \quad * \mathsf{uninit}(q + \mathtt{numreaders}) * \ \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del})\end{array}\right\}$

$\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, 0, \emptyset) * \Box(\Gamma.q = q) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{wcounter}) * \mathsf{uninit}(q + \mathtt{link}) \\ \quad * \mathsf{uninit}(q + \mathtt{numreaders}) * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del})\end{array}\right\}$

$[q + \mathtt{link}]_{\mathtt{at}} := 0;$

$\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, 0, \emptyset) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \Box\left(\boxed{q + \mathtt{link} : (0 \cdot \mathtt{nil}, \mathsf{null} \cdot \mathtt{nil}) \mid \mathbf{LLP}(\Gamma, q, j)}\right) \\ \quad * \Box(\mathsf{SnapshotValid}(\mathtt{alloc}(0, q, \mathsf{null}))) * \mathsf{uninit}(q + \mathtt{wcounter}) * \mathsf{uninit}(q + \mathtt{numreaders}) * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del})\end{array}\right\}$

$[q + \mathtt{wcounter}]_{\mathtt{at}} := 0;$

$\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, 0, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \Box\left(\boxed{q + \mathtt{wcounter} : (\mathtt{alloc}(0, q, \mathsf{null}), 0) \mid \mathbf{WCP}(\Gamma)}\right) \\ \quad * \mathsf{uninit}(q + \mathtt{numreaders}) * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del})\end{array}\right\}$

$\mathtt{let}\ sc = \mathtt{alloc}(1) \quad$ *`/* Scratch space for counter – leaks memory */`*

$\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, 0, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * \mathsf{uninit}(sc)\end{array}\right\}$

$[sc]_{\mathtt{na}} := 0;$

$\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, 0, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * sc \hookrightarrow 0\end{array}\right\}$

$\left\{\begin{array}{l}\exists c.\, \mathsf{RCountersInitUpTo}(\Gamma, 0, c, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * sc \hookrightarrow c\end{array}\right\}$

`repeat`

  $\mathtt{let}\ i = [sc]_{\mathtt{na}}$

  $\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, i, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * sc \hookrightarrow i\end{array}\right\}$

  $[q + \mathtt{rcounters} + i]_{\mathtt{at}} := 0$

  $\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, i + 1, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * sc \hookrightarrow i\end{array}\right\}$

  $[sc]_{\mathtt{na}} := i + 1;$

  $\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, i + 1, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * sc \hookrightarrow i + 1\end{array}\right\}$

  $i + 1 == N$

`end;`

$\left\{\begin{array}{l}\mathsf{RCountersInitUpTo}(\Gamma, 0, N, \{0\}) * \boxed{j : \mathrm{Master}(0 \cdot \mathtt{nil})} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del})\end{array}\right\}$

$\left\{\begin{array}{l}\left(\ast_{tid<N} \mathsf{ReaderSafe}(q, H, tid)\right) * \boxed{j : \mathrm{Master}_N(0 \cdot \mathtt{nil})} * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(\mathtt{alloc}(0, q, \mathsf{null}))} * \mathsf{uninit}(q + \mathtt{numreaders}) \\ \quad * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N\} \times \mathbb{N}} * \boxed{\Gamma.\mathsf{ctok} : \{N\} \times (\mathbb{N} \setminus \{0\})}\end{array}\right\}$

$[q + \mathtt{numreaders}]_{\mathtt{at}} := 0;$

$\left\{\begin{array}{l}\Box\left(\boxed{q + \mathtt{numreaders} : (\mathtt{alloc}(0, q, \mathsf{null}), 0) \mid \mathbf{NRP}(\Gamma)}\right) * \boxed{j : \mathrm{Master}_N(0 \cdot \mathtt{nil})} * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(\mathtt{alloc}(0, q, \mathsf{null}))} \\ \quad * \mathsf{uninit}(q + \mathtt{numreaders}) * \mathsf{uninit}(q + \mathtt{free}) * \mathsf{uninit}(q + \mathtt{del}) * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N\} \times \mathbb{N}} * \boxed{\Gamma.\mathsf{ctok} : \{N\} \times (\mathbb{N} \setminus \{0\})}\end{array}\right\}$

$[q + \mathtt{del}]_{\mathtt{na}} := \mathtt{newStack}();$

$[q + \mathtt{free}]_{\mathtt{na}} := \mathtt{newStack}();$

$$\left\{\begin{array}{l}\mathsf{Stack}(q+\texttt{del},\texttt{nil})*\mathsf{Stack}(q+\texttt{free},\texttt{nil})*\mathsf{NoDup}(\texttt{nil})*\mathsf{DeadFrom}(\texttt{nil},\texttt{nil},\texttt{alloc}(0,q,\mathsf{null}),\texttt{alloc}(0,q,\mathsf{null}))\\ \quad *\boxed{\Gamma.\mathsf{history}:\mathrm{Master}(\texttt{alloc}(0,q,\mathsf{null}))}*\boxed{\Gamma.\mathsf{rxtok}:\{N\}\times\mathbb{N}}*\boxed{\Gamma.\mathsf{wxtok}:\{0,\ldots,N\}\times\mathbb{N}}\\ \quad *\boxed{\Gamma.\mathsf{ctok}:\{N\}\times(\mathbb{N}\setminus\{0\})}*\mathsf{TraceSpine}(\Gamma,\texttt{alloc}(0,q,\mathsf{null}),(q,\mathsf{null})\cdot\texttt{nil})\end{array}\right\}$$
$$\left\{\mathsf{WriterSafe}(q,(q,\mathsf{null})\cdot\texttt{nil})\right\}$$
$$q$$
$$\left\{q.\,\mathsf{WriterSafe}'(q,q+\texttt{link}\cdot\texttt{nil})*\mathsf{ReaderQueue}(q)\right\}$$

C.4.2 Verification of `registerReader`

$$\left\{\mathsf{ReaderQueue}(q)\right\}$$
$$\texttt{registerReader}(q)$$
$$\left\{x.\,\exists H.\,(x<N*\mathsf{ReaderSafe}(q,H,x))\vee(x\geq N)\right\}$$

This function consists of a single FAI. The key is that when we perform the FAI, if the current value v is less than N, then there is a $\mathsf{ReaderSafe}(\Gamma,H,v)$ stored in the protocol, which the reader is allowed to take out as part of the FAI.

C.4.3 Verification of `rcuReadNext`

$$\left\{\exists p.\,\mathsf{ReaderSafe}(q,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow -\right\}$$
$$\texttt{rcuReadNext}(q,nextptr,retptr)$$
$$\left\{x.\,\exists v,p.\,\mathsf{ReaderSafe}(q,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow v*((x=0\wedge P(v))\vee x=1)\right\}$$

First, as a technicality, note that:

$$\mathsf{SnapshotValid}(\Gamma,H)*\mathsf{SnapshotValid}(\Gamma',H)\Rightarrow\Gamma=\Gamma'$$

To see this, note that SnapshotValid implies H is non-empty and $H_*(\Gamma.q)=\mathsf{base}(H)\cdot\texttt{nil}$ and $H^*(\mathsf{base}(H))\neq\top$, hence we have that $\boxed{\Gamma.q+\texttt{link}:(H_*(\Gamma.q),H^*_*(q))\,|\,\mathbf{LLP}(\Gamma,q,j)}$ and $\boxed{\Gamma.q+\texttt{link}:(H_*(\Gamma.q),H^*_*(q))\,|\,\mathbf{LLP}(\Gamma',q,j)}$, so the rules for separation of protocol assertions guarantees that $\mathbf{LLP}(\Gamma,q,j)=\mathbf{LLP}(\Gamma',q,j)$, hence $\Gamma=\Gamma'$.

$$\left\{\exists p.\,\mathsf{ReaderSafe}(q,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow -\right\}$$
$$\texttt{let}\ p=[nextptr]_{\texttt{na}}$$
$$\left\{\mathsf{ReaderSafe}(q,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow -\right\}$$
$$\left\{\exists\Gamma.\,\Gamma.q=q*\mathsf{AccessList}(\Gamma,H,tid)*\mathsf{RCounterValid}(\Gamma,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow -\right\}$$
$$\left\{\Box(\Gamma.q=q)*\mathsf{AccessList}(\Gamma,H,tid)*\mathsf{RCounterValid}(\Gamma,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow -\right\}$$
$$\left\{\begin{array}{l}\Box(\mathsf{SnapshotValid}(\Gamma,H))*\boxed{\Gamma.\mathsf{rxtok}:\{tid\}\times(\mathbb{N}\setminus\mathsf{dead}(H))}\\ \quad *\exists j.\,\boxed{\Gamma.q+\texttt{link}:(\mathsf{base}(H)\cdot\texttt{nil},H(\mathsf{base}(H)))\,|\,\mathbf{LLP}(\Gamma,q,j)}*\boxed{j:\mathrm{Master}_{tid}(\mathsf{base}(H)\cdot\texttt{nil})}\\ \quad *\mathsf{RCounterValid}(\Gamma,H,tid)*nextptr\hookrightarrow p*\mathsf{SafePtr}(H,p)*retptr\hookrightarrow -\end{array}\right\}$$
$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{rxtok}:\{tid\}\times(\mathbb{N}\setminus\mathsf{dead}(H))}*\ \mathsf{RCounterValid}(\Gamma,H,tid)*nextptr\hookrightarrow p*retptr\hookrightarrow -\\ \quad *\exists j.\,\boxed{\Gamma.q+\texttt{link}:(\mathsf{base}(H)\cdot\texttt{nil},H(\mathsf{base}(H)))\,|\,\mathbf{LLP}(\Gamma,q,j)}*\boxed{j:\mathrm{Master}_{tid}(\mathsf{base}(H)\cdot\texttt{nil})}\\ \quad *\exists\Gamma'.\,\mathsf{SnapshotValid}(\Gamma',H)*((p=0)\vee(p\neq0*\exists i.\,i\notin\mathsf{dead}(H)*\mathsf{PermX}(\Gamma',p,tid,i)))\end{array}\right\}$$
$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{rxtok}:\{tid\}\times(\mathbb{N}\setminus\mathsf{dead}(H))}*\ \mathsf{RCounterValid}(\Gamma,H,tid)*nextptr\hookrightarrow p*retptr\hookrightarrow -\\ \quad *\Box\left(\boxed{\Gamma.q+\texttt{link}:(\mathsf{base}(H)\cdot\texttt{nil},H(\mathsf{base}(H)))\,|\,\mathbf{LLP}(\Gamma,q,j)}\right)*\boxed{j:\mathrm{Master}_{tid}(\mathsf{base}(H)\cdot\texttt{nil})}\\ \quad *\ ((p=0)\vee(p\neq0*\exists i.\,i\notin\mathsf{dead}(H)*\mathsf{PermX}(\Gamma,p,tid,i)))\end{array}\right\}$$
$$\texttt{if}\ p\ \texttt{==}\ 0\ \texttt{then}\ 1$$
$$\texttt{else}$$
$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{rxtok}:\{tid\}\times(\mathbb{N}\setminus\mathsf{dead}(H))}*\mathsf{RCounterValid}(\Gamma,H,tid)*\boxed{j:\mathrm{Master}_{tid}(\mathsf{base}(H)\cdot\texttt{nil})}*nextptr\hookrightarrow p*retptr\hookrightarrow -\\ \quad *\exists i.\,i\notin\mathsf{dead}(H)*\mathsf{PermX}(\Gamma,p,tid,i)\end{array}\right\}$$

$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times (\mathbb{N} \setminus \mathsf{dead}(H))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})} * nextptr \hookrightarrow p * retptr \hookrightarrow - \right.$$
$$\left. \quad * \square(i \notin \mathsf{dead}(H) * \mathsf{PermX}(\Gamma, p, tid, i)) \right\}$$
$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times ((\mathbb{N} \setminus \mathsf{dead}(H) \setminus \{i\}))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad \left((\exists v.\, p + \texttt{data} \overset{tid}{\hookrightarrow} v * P(v)) * (\exists j_p, L.\, \boxed{p + \texttt{link} : (i \cdot L, -) \mid \mathbf{LLP}(\Gamma, p, j_p)} * \boxed{j_p : \mathrm{Master}_{tid}(i \cdot L)})\right)\right.$$
$$\left. \quad * nextptr \hookrightarrow p * retptr \hookrightarrow - \right\}$$
$$\texttt{let } v = [p + \texttt{data}]_{\texttt{na}}$$
$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times ((\mathbb{N} \setminus \mathsf{dead}(H) \setminus \{i\}))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad p + \texttt{data} \overset{tid}{\hookrightarrow} v * P(v) * \boxed{p + \texttt{link} : (i \cdot L, -) \mid \mathbf{LLP}(\Gamma, p, j_p)} * \boxed{j_p : \mathrm{Master}_{tid}(i \cdot L)}\right.$$
$$\left. \quad * nextptr \hookrightarrow p * retptr \hookrightarrow - \right\}$$
$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times ((\mathbb{N} \setminus \mathsf{dead}(H) \setminus \{i\}))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad p + \texttt{data} \overset{tid}{\hookrightarrow} v * \square(P(v)) * nextptr \hookrightarrow p * retptr \hookrightarrow - \right.$$
$$\left. \quad \exists i', L'.\, \boxed{p + \texttt{link} : (i \cdot L, i' \cdot L') \mid \mathbf{LLP}(\Gamma, p, j_p)} * (p \notin \mathrm{dom}(H_*) \vee H_*(p) < i \cdot L \vee (H_*(p) = i \cdot L \wedge H^*(i) \leq i' \cdot L')) \right.$$
$$\left. \quad * \boxed{j_p : \mathrm{Master}_{tid}(i \cdot L)} \right\}$$
$$\texttt{let } p' = [p + \texttt{link}]_{\texttt{at}}$$
$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times ((\mathbb{N} \setminus \mathsf{dead}(H) \setminus \{i\}))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad * nextptr \hookrightarrow p * retptr \hookrightarrow - p + \texttt{data} \overset{tid}{\hookrightarrow} v * \boxed{j_p : \mathrm{Master}_{tid}(i \cdot L)} \right.$$
$$\left. \quad * ((p' \neq 0 * \exists i'', L''.\, \boxed{p + \texttt{link} : (i \cdot L, i'' \cdot L'') \mid \mathbf{LLP}(\Gamma, p, j)} * \exists H'.\, \boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H')} * i'' \notin \mathsf{dead}(H) \right.$$
$$\left. \quad\quad * H'(i) = i'' \cdot L'' * \forall tid < N.\mathsf{PermX}(\Gamma, p', tid, i'')) \vee (p' = 0)) \right\}$$
$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times ((\mathbb{N} \setminus \mathsf{dead}(H)))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad * nextptr \hookrightarrow p * retptr \hookrightarrow - * \mathsf{SafePtr}(q, H, p') \right\}$$
$$[retptr]_{\texttt{na}} := v;$$
$$[nextptr]_{\texttt{na}} := p';$$
$$\left\{\boxed{\Gamma.\texttt{rxtok} : \{tid\} \times ((\mathbb{N} \setminus \mathsf{dead}(H)))} * \mathsf{RCounterValid}(\Gamma, H, tid) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad * nextptr \hookrightarrow p' * retptr \hookrightarrow v * \mathsf{SafePtr}(q, H, p') \right\}$$
$$\left\{\mathsf{ReaderSafe}(q, H, tid) * nextptr \hookrightarrow p' * \mathsf{SafePtr}(q, H, p') * retptr \hookrightarrow v * P(v)\right\}$$
$$0$$
$$\left\{x.\, \exists v, p.\, \mathsf{ReaderSafe}(q, H, tid) * nextptr \hookrightarrow p * \mathsf{SafePtr}(H, p) * retptr \hookrightarrow v * ((x = 0 \wedge P(v)) \vee x = 1)\right\}$$

C.4.4 Verification of `rcuReadStart`

At this point we also justify the rule:

$$\left\{\mathsf{ReaderSafe}(q, H, tid)\right\}[q + \texttt{link}]_{\texttt{at}}\left\{p.\ \mathsf{ReaderSafe}(q, H, tid) * \mathsf{SafePtr}(q, H, p)\right\}$$

since this is what allows us to first get a SafePtr with which we can call `rcuReadNext`.

$$\left\{\mathsf{ReaderSafe}(q, H, tid)\right\}$$
$$\left\{\exists \Gamma.\, \Gamma.q = q * \mathsf{AccessList}(\Gamma, H, tid) * \mathsf{RCounterValid}(\Gamma, H, tid)\right\}$$
$$\left\{\square(\Gamma.q = q) * \mathsf{AccessList}(\Gamma, H, tid) * \mathsf{RCounterValid}(\Gamma, H, tid)\right\}$$
$$\left\{\square(\mathsf{SnapshotValid}(\Gamma, H)) * \square(H \neq \texttt{nil}) * \square\left(\boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H)}\right) * \square(\mathsf{base}(H) \notin \mathsf{dead}(H))\right.$$
$$\left. \quad * \exists j.\, \boxed{\Gamma.q + \texttt{link} : (\mathsf{base}(H) \cdot \texttt{nil}, H(\mathsf{base}(H))) \mid \mathbf{LLP}(\Gamma, q, j)} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad * \boxed{\Gamma.\texttt{rxtok} : \{tid\} \times \{\mathbb{N} \setminus \mathsf{dead}(H)\}} * \mathsf{RCounterValid}(\Gamma, H, tid) \right\}$$
$$\left\{\square\left(\boxed{\Gamma.q + \texttt{link} : (\mathsf{base}(H) \cdot \texttt{nil}, H(\mathsf{base}(H))) \mid \mathbf{LLP}(\Gamma, q, j)}\right) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H) \cdot \texttt{nil})}\right.$$
$$\left. \quad * \boxed{\Gamma.\texttt{rxtok} : \{tid\} \times \{\mathbb{N} \setminus \mathsf{dead}(H)\}} * \mathsf{RCounterValid}(\Gamma, H, tid) \right\}$$
$$[q + \texttt{link}]_{\texttt{at}}$$

$$\left\{\begin{array}{l} p.\boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H)\cdot \mathtt{nil})} * \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H))} * \mathsf{RCounterValid}(\Gamma, H, tid) \\ \quad * ((p\neq 0 * \exists i'', L''.\boxed{q + \mathtt{link} : (i\cdot L, i''\cdot L'')\mid \mathbf{LLP}(\Gamma, q, i)} * i''\notin \mathsf{dead}(H) \\ \quad\quad * \exists H'.\boxed{\Gamma.\mathsf{history} : \mathrm{Snapshot}(H')} * H'(i) = i''\cdot L'' * \forall tid < N.\mathsf{PermX}(\Gamma, p, tid, i'')) \vee (p = 0)) \end{array}\right\}$$
$$\left\{p.\,\mathsf{ReaderSafe}(q, H, tid) * \mathsf{SafePtr}(q, H, p)\right\}$$

C.4.5 Verification of `rcuQuiescentState`

$$\left\{\exists H.\,\mathsf{ReaderSafe}(q, H, tid)\right\}$$
$$\quad \mathtt{rcuQuiescentState}(q, tid)$$
$$\left\{\exists H'.\,\mathsf{ReaderSafe}(q, H', tid)\right\}$$

Notice that we could give this spec to a function which did nothing. Because we don't prove liveness properties, this spec doesn't guarantee that the writer can make progress, even if the readers do call `rcuQuiescentState`.

$$\left\{\exists H.\,\mathsf{ReaderSafe}(q, H, tid)\right\}$$
$$\left\{\mathsf{ReaderSafe}(q, H, tid)\right\}$$
$$\left\{\exists \Gamma.\,\Gamma.q = q * \mathsf{AccessList}(\Gamma, H, tid) * \mathsf{RCounterValid}(\Gamma, H, tid)\right\}$$
$$\left\{\square(\Gamma.q = q) * \mathsf{AccessList}(\Gamma, H, tid) * \mathsf{RCounterValid}(\Gamma, H, tid)\right\}$$
$$\left\{\begin{array}{l} \mathsf{SnapshotValid}(\Gamma, H) * \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H))} \\ \quad * \exists j.\,\boxed{\Gamma.q + \mathtt{link} : (\mathsf{base}(H)\cdot \mathtt{nil}, H(\mathsf{base}(H)))\mid \mathbf{LLP}(\Gamma, q, j)} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H)\cdot \mathtt{nil})} \\ \quad * \exists v_1, v_2, H'.\,(H', v_1)\leq (H, v_2) * \boxed{\Gamma.q + \mathtt{wcounter} : (H, v_2)\mid \mathbf{WCP}(\Gamma)} * \boxed{\Gamma.q + \mathtt{rcounters} + tid : (H', v_1)\mid \mathbf{RCP}(\Gamma, tid)} \\ \quad\quad * \boxed{\Gamma.\mathsf{ctok} : \{tid\}\times(\mathbb{N}\setminus\{0,\ldots,v_1\})} * (\forall i\in \mathsf{dead}(H).\,\mathsf{ModX}(\Gamma, tid, i)) \end{array}\right\}$$
$$\left\{\begin{array}{l} \square(\mathsf{SnapshotValid}(\Gamma, H)) * \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H))} \\ \quad \square\left(\boxed{\Gamma.q + \mathtt{link} : (\mathsf{base}(H)\cdot \mathtt{nil}, H(\mathsf{base}(H)))\mid \mathbf{LLP}(\Gamma, q, j)}\right) * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H)\cdot \mathtt{nil})} \\ \quad * \square((H', v_1)\leq (H, v_2)) * \square\left(\boxed{\Gamma.q + \mathtt{wcounter} : (H, v_2)\mid \mathbf{WCP}(\Gamma)}\right) * \square\left(\boxed{\Gamma.q + \mathtt{rcounters} + tid : (H', v_1)\mid \mathbf{RCP}(\Gamma, tid)}\right) \\ \quad\quad * \boxed{\Gamma.\mathsf{ctok} : \{tid\}\times(\mathbb{N}\setminus\{0,\ldots,v_1\})} * \square((\forall i\in \mathsf{dead}(H).\,\mathsf{ModX}(\Gamma, tid, i))) \end{array}\right\}$$
$\mathtt{let}\ t = [q + \mathtt{wcounter}]_{\mathtt{at}}$
$$\left\{\begin{array}{l} \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H))} * \boxed{\Gamma.\mathsf{ctok} : \{tid\}\times(\mathbb{N}\setminus\{0,\ldots,v_1\})} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H)\cdot \mathtt{nil})} \\ \quad * \exists H'', v_3.\,t = v_3 * (H, v_2)\leq (H'', v_3) * \boxed{q + \mathtt{wcounter} : (H'', v_3)\mid \mathbf{WCP}(\Gamma)} * \mathsf{SnapshotValid}(\Gamma, H'') \end{array}\right\}$$
$$\left\{\begin{array}{l} \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H))} * \boxed{\Gamma.\mathsf{ctok} : \{tid\}\times(\mathbb{N}\setminus\{0,\ldots,v_1 - 1\})} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H)\cdot \mathtt{nil})} \\ \quad * \square(t = v_3) * \square((H, v_2)\leq (H'', v_3)) * \square\left(\boxed{q + \mathtt{wcounter} : (H'', v_3)\mid \mathbf{WCP}(\Gamma)}\right) * \square(\mathsf{SnapshotValid}(\Gamma, H'')) \end{array}\right\}$$
$$\left\{\begin{array}{l} \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H''))} * \boxed{\Gamma.\mathsf{ctok} : \{tid\}\times(\mathbb{N}\setminus\{0,\ldots,v_1\})} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H'')\cdot \mathtt{nil})} \\ \quad * \square(\mathsf{base}(H) = \mathsf{base}(H'')) * \square(\forall i\in \mathsf{dead}(H'').\,\mathsf{ModX}(\Gamma, tid, i)) \end{array}\right\}$$
$[q + \mathtt{rcounters} + tid]_{\mathtt{at}} := t;$
$$\left\{\begin{array}{l} \boxed{\Gamma.\mathsf{rxtok} : \{tid\}\times(\mathbb{N}\setminus \mathsf{dead}(H''))} * \boxed{\Gamma.\mathsf{ctok} : \{tid\}\times(\mathbb{N}\setminus\{0,\ldots,v_3\})} * \boxed{j : \mathrm{Master}_{tid}(\mathsf{base}(H'')\cdot \mathtt{nil})} \\ \quad * \square\left(\boxed{q + \mathtt{rcounters} + tid : (H'', v_3)\mid \mathbf{RCP}(\Gamma, tid)}\right) \end{array}\right\}$$
$$\left\{\mathsf{ReaderSafe}(q, H'', tid)\right\}$$
0
$$\left\{\exists H.\,\mathsf{ReaderSafe}(\Gamma, H, tid)\right\}$$

C.4.6 Verification of `rcuCollect`

This routine collects tokens for dead nodes from currently registered readers upto reader id n. It is called by `rcuSynchronize`, which collects the tokens of the unregistered readers via a read-modify-write on $q + \texttt{numreaders}$. The specification and proof are parameterized by two traces, H_1 and H_2 (that is, we are proving here a family of triples). We exchange the wxtok for rxtok for each i which is dead in H_2 but not H_1.

$$\left\{\begin{array}{l}\Gamma.q = q * \boxed{q + \texttt{wcounter} : (H_2, newgc) \mid \mathsf{WCP}(\Gamma)} * H_1 \le H_2 * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * n > 0 \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \forall tid < n. \boxed{q + \texttt{rcounters} + tid : - \mid \mathsf{RCP}(\Gamma, tid)}\end{array}\right\}$$

$\texttt{rcuCollect}(q, n, newgc)$

$$\left\{\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{rxtok} : \{0,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\right\}$$

$$\left\{\begin{array}{l}\Box(\Gamma.q = q) * \Box\left(\boxed{q + \texttt{wcounter} : (H_2, newgc) \mid \mathsf{WCP}(\Gamma)}\right) * \Box(H_1 \le H_2) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \Box(n > 0) \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \Box\left(\forall tid < n. \boxed{q + \texttt{rcounters} + tid : - \mid \mathsf{RCP}(\Gamma, tid)}\right)\end{array}\right\}$$

$\texttt{let } sc = \texttt{alloc}(1)$

$[sc]_{\mathtt{na}} := 0;$

$$\left\{\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * sc \hookrightarrow 0\right\}$$

$$\left\{\begin{array}{l}\exists k. \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow k * k < n \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{k,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,k-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

`repeat` *`/* somewhat awkward because there is no for loop primitive */`*

`let` $i = [sc]_{\mathtt{na}}$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow i * \Box(i < n) \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,i-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

`repeat` $[q + \texttt{rcounters} + i]_{\mathtt{at}} == newgc$ `end`

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow i \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,i-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \exists H', v'. v' = newgc * \boxed{q + counter : (H', v') \mid \mathsf{WCP}(\Gamma)} \\ \qquad * (\forall i \in \mathsf{dead}(H'). \boxed{\Gamma.\mathsf{rxtok} : \{(tid, i)\}} \vee \boxed{\Gamma.\mathsf{wxtok} : \{(tid, i)\}})\end{array}\right\}$$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow i \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,i-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \Box(v' = newgc) * \Box\left(\boxed{q + counter : (H', v') \mid \mathsf{WCP}(\Gamma)}\right) * (H_2, newgc) \le (H, v') \vee (H, v') \le (H_2, newgc) \\ \qquad * \Box(\forall i \in \mathsf{dead}(H'). \mathsf{ModX}(\Gamma, tid, i))\end{array}\right\}$$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow i \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,i-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * H_2 = H'\end{array}\right\}$$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow i \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i+1,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,i\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$[sc]_{\mathtt{na}} := i + 1;$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow i + 1 \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i+1,\dots,n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0,\dots,i\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$i + 1 == n$

`end;`

$$\left\{\begin{array}{l}\exists i.\ \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * i + 1 = n * sc \hookrightarrow i \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{i, \ldots, n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, i-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$$\left\{\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * sc \hookrightarrow n-1 * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\right\}$$

$\mathtt{free}(sc)$;

$$\left\{\boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\right\}$$

0

C.4.7 Verification of `rcuSynchronize`

The specification and proof are parameterized by two traces, H_1 and H_2 (that is, we are proving here a family of triples). `rcuSynchronize` exchanges all of the wxtok for rxtok for each i which is dead in H_2 but not H_1. In `rcuNodeUpdate`, this will be instantiated to some particular H_1 and H_2, and then the caller will use the rxtok to get access to the node it wants to deallocate.

$$\left\{\exists \Gamma.\, \Gamma.q = q * H_1 \le H_2 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{SnapshotValid}(\Gamma, H_2) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)}\right\}$$

$\mathtt{rcuSynchronize}(q)$

$$\left\{\exists \Gamma.\, \Gamma.q = q * \mathsf{RevokedUpTo}(\Gamma, H_2) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\right\}$$

$$\left\{\exists \Gamma.\, \Gamma.q = q * \mathsf{RevokedUpTo}(\Gamma, H_1) * H_1 \le H_2 * \mathsf{SnapshotValid}(\Gamma, H_2) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)}\right\}$$

$$\left\{\Box(\Gamma.q = q) * \mathsf{RevokedUpTo}(\Gamma, H_1) * \Box(H_1 \le H_2) * \Box(\mathsf{SnapshotValid}(\Gamma, H_2)) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)}\right\}$$

$$\left\{\begin{array}{l}\exists v_1, v_2.\ \boxed{q + \mathtt{wcounter} : (H_1, v_1) \mid \mathsf{WCP}(\Gamma)} * \boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1\}} * \boxed{q + \mathtt{numreaders} : (H_2, v_2) \mid \mathsf{NRP}(\Gamma)} \\ \quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$$\left\{\begin{array}{l}\Box\left(\boxed{q + \mathtt{wcounter} : (H_1, v_1) \mid \mathsf{WCP}(\Gamma)}\right) * \boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1\}} * \Box\left(\boxed{q + \mathtt{numreaders} : (H_2, v_2) \mid \mathsf{NRP}(\Gamma)}\right) \\ \quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \mathsf{AccessList}(\Gamma, H_1, N)\end{array}\right\}$$

$\mathtt{let}\ oldgc = [q + \mathtt{wcounter}]_{\mathtt{at}}$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1\}} * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \mathsf{AccessList}(\Gamma, H_1, N) * \Box(oldgc = v_1)\end{array}\right\}$$

$\mathtt{let}\ newgc = oldgc + 1$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1\}} * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \mathsf{AccessList}(\Gamma, H_1, N) * \Box(newgc = v_1 + 1)\end{array}\right\}$$

$[q + \mathtt{wcounter}]_{\mathtt{at}} := newgc$;

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1 + 1\}} * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, N-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \mathsf{AccessList}(\Gamma, H_1, N) * \Box\left(\boxed{q + \mathtt{wcounter} : (H_2, v_1 + 1) \mid \mathsf{WCP}(\Gamma)}\right)\end{array}\right\}$$

$\mathtt{let}\ n = \mathtt{FAI}(q + \mathtt{numreaders}, 0)$ *`/* Fetch and increment by 0 */`*

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1 + 1\}} * \Box\left(\boxed{q + \mathtt{numreaders} : (H_2, n) \mid \mathsf{NRP}(\Gamma)}\right) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{rxtok} : \{n, \ldots, N\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \mathsf{AccessList}(\Gamma, H_2, N) * \forall tid < N.\ \boxed{q + \mathtt{rcounters} + tid : - \mid \mathsf{RCP}(\Gamma, tid)}\end{array}\right\}$$

$\mathtt{if}\ n == 0\ \mathtt{then}\ 0$

$\mathtt{else}$

$$\left\{\begin{array}{l}\boxed{\Gamma.\mathsf{ctok} : \{N\} \times \{\mathbb{N} \setminus 0, \ldots, v_1 + 1\}} * \Box\left(\boxed{q + \mathtt{numreaders} : (H_2, n) \mid \mathsf{NRP}(\Gamma)}\right) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} \\ \quad * \boxed{\Gamma.\mathsf{wxtok} : \{0, \ldots, n-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} * \boxed{\Gamma.\mathsf{rxtok} : \{n, \ldots, N\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))} \\ \quad * \mathsf{AccessList}(\Gamma, H_2, N) * \forall tid < N.\ \boxed{q + \mathtt{rcounters} + tid : - \mid \mathsf{RCP}(\Gamma, tid)} * \Box(n > 0)\end{array}\right\}$$

$\mathtt{rcuCollect}(q, n, newgc)$

$$\left\{\mathsf{RevokedUpTo}(\Gamma, H_2) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\right\}$$

0

$\left\{\exists \Gamma.\, \Gamma.q = q * \mathsf{RevokedUpTo}(\Gamma, H_2) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_2)} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N-1\} \times (\mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1))}\right\}$

C.4.8 Verification of `rcuAlloc`

$\{\Gamma.q = q * \mathsf{FreeValid}(\Gamma)\}$

`rcuAlloc`(q)

$\left\{p.\, ((\exists S, j.\, \boxed{p + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, p, j)} * \boxed{j : \mathrm{Master}(S)} * p + \mathtt{data} \hookrightarrow -) \vee (\mathsf{uninit}(p + \mathtt{link}) * \mathsf{uninit}(p + \mathtt{data}))) \right.$
$\left. \quad * \mathsf{FreeValid}(\Gamma)\right\}$

$\left\{\square(\Gamma.q = q) * \mathsf{FreeValid}(\Gamma)\right\}$

$\left\{\exists L.\, \mathsf{Stack}(\Gamma.q + \mathtt{free}, L) * (\mathop{\Large *}_{i<|L|} \exists j, S.\, \boxed{L[i] + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L[i], j)} * \boxed{j : \mathrm{Master}(S)} * L[i] + \mathtt{data} \hookrightarrow -)\right\}$

$\left\{\mathsf{Stack}(q + \mathtt{free}, L) * (\mathop{\Large *}_{i<|L|} \exists j, S.\, \boxed{L[i] + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L[i], j)} * \boxed{j : \mathrm{Master}(S)} * L[i] + \mathtt{data} \hookrightarrow -)\right\}$

`let` $p =$ `pop`$(q + \mathtt{free})$

$\left\{((p = 0 * L = \mathtt{nil} * \mathsf{Stack}(q + \mathtt{free}, \mathtt{nil})) \vee (p \neq 0 * L = L' \cdot i' * \mathsf{Stack}(q + \mathtt{free}, L') * p = L[i'])) \right.$
$\left. \quad *(\mathop{\Large *}_{i<|L|} \exists j, S.\, \boxed{L[i] + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L[i], j)} * \boxed{j : \mathrm{Master}(S)} * L[i] + \mathtt{data} \hookrightarrow -))\right\}$

`if` p `==` 0 `then` `alloc`(2)

`else`

$\left\{\square(p \neq 0) * \square(L = L' \cdot i') * \mathsf{Stack}(q + \mathtt{free}, L') * \square(p = L[i']) \right.$
$\left. \quad *(\mathop{\Large *}_{i<|L|} \exists j, S.\, \boxed{L[i] + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L[i], j)} * \boxed{j : \mathrm{Master}(S)} * L[i] + \mathtt{data} \hookrightarrow -))\right\}$

$\left\{(\exists j, S.\, \boxed{p + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, p, j)} * \boxed{j : \mathrm{Master}(S)} * p + \mathtt{data} \hookrightarrow - * \mathsf{Stack}(q + \mathtt{free}, L') \right.$
$\left. \quad *(\mathop{\Large *}_{i<|L'|} \exists j, S.\, \boxed{L'[i] + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, L'[i], j)} * \boxed{j : \mathrm{Master}(S)} * L'[i] + \mathtt{data} \hookrightarrow -))\right\}$

$\left\{(\exists j, S.\, \boxed{p + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, p, j)} * \boxed{j : \mathrm{Master}(S)} * p + \mathtt{data} \hookrightarrow - * \mathsf{FreeValid}(\Gamma))\right\}$

p

$\left\{p.\, ((\exists S, j.\, \boxed{p + \mathtt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, p, j)} * \boxed{j : \mathrm{Master}(S)} * p + \mathtt{data} \hookrightarrow -) \vee (\mathsf{uninit}(p + \mathtt{link}) * \mathsf{uninit}(p + \mathtt{data}))) \right.$
$\left. \quad * \mathsf{FreeValid}(\Gamma)\right\}$

C.4.9 Verification of `rcuDealloc`

$\left\{\Gamma.q = q * H_1 \leq H_2 \leq H_3 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{SnapshotValid}(\Gamma, H_3) \right.$
$\quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \exists i.\, i \in \mathsf{dead}(H_3) \setminus \mathsf{dead}(H_2) * H_{3*}(x) = i \cdot - * (\forall n < N.\, \mathsf{PermX}(\Gamma, x, n, i))$
$\left. \quad * \exists j.\, \boxed{x + \mathtt{link} : (H_{3*}(x), -) \mid \mathbf{LLP}(\Gamma, x, j)} * \boxed{j : \mathrm{Master}_N(H_{3*}(x))} * x + \mathtt{data} \overset{N}{\hookrightarrow} -\right\}$

`rcuDealloc`(q, x)

$\left\{\exists H_1.\, H_1 \leq H_3 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_3) * \mathsf{FreeValid}(\Gamma) \right.$
$\left. \quad * \mathsf{SnapshotValid}(\Gamma, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)}\right\}$

There are a few subtle points in this proof that are not clear from the Hoare triple outline. First, the input x is pushed onto $q + \mathtt{del}$. This extends $\mathsf{DeallocBetween}(\Gamma, H_1, H_2)$ to $\mathsf{DeallocBetween}(\Gamma, H_1, H_3)$, since the abstract location associated with x is dead in H_3 but not H_2. This predicate says that there is some list L_d of locations stored in the stack at $q + \mathtt{del}$ and an associated list L'_d of abstract locations matching the physical locations. To extend this to now be about the list $L_d \cdot x$ and $L_d \cdot i$, we first need to show that $x \notin L_d$ and $i \notin L'_d$ (to satisfy the NoDup predicates in both). We know $x \notin L_d$, since if it were, by $\mathsf{DeadFrom}(\Gamma, L_d, L'_d, H_1, H_2)$ we would have a second copy of $x + \mathtt{data} \overset{N}{\hookrightarrow} -$, which is a contradiction. Second, we know that $i \notin L'_d$, since if it were, we would have that $i \in \mathsf{dead}(H_2) \setminus \mathsf{dead}(H_1)$, but we also know from the precondition to `rcuDealloc` that $i \in \mathsf{dead}(H_3) \setminus \mathsf{dead}(H_2)$, which is a contradiction. Finally, the writer moves the fractional permissions for $x + \mathtt{data}$ and the master ghost state related to the protocol of $x + \mathtt{link}$ into the DeadFrom predicate to establish $\mathsf{DeadFrom}(L_d \cdot x, L'_d \cdot i, H_1, H_3)$.

$$\left\{\begin{array}{l}\square(\Gamma.q = q) * \square(H_1 \le H_2 \le H_3) * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \square(\mathsf{SnapshotValid}(\Gamma, H_3)) \\ \quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \square(i \in \mathsf{dead}(H_3) \setminus \mathsf{dead}(H_2) * H_{3*}(x) = i \cdot - * (\forall n < N.\, \mathsf{PermX}(\Gamma, x, n, i))) \\ \quad * \square\left(\boxed{x + \texttt{link} : (H_{3*}(x), -) \mid \mathbf{LLP}(\Gamma, x, j)}\right) * \boxed{j : \mathrm{Master}_N(H_{3*}(x))} * x + \texttt{data} \overset{N}{\hookrightarrow} -\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} \\ \quad * \boxed{j : \mathrm{Master}_N(H_{3*}(x))} * x + \texttt{data} \overset{N}{\hookrightarrow} -\end{array}\right\}$$

$\texttt{push}(q + \texttt{del}, x)$

$$\left\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_3) * \mathsf{FreeValid}(\Gamma) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)}\right\}$$

$\texttt{let } c = \texttt{choose}(1, 2)$

$\texttt{if } c == 1 \texttt{ then}$

0

$$\left\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_3) * \mathsf{FreeValid}(\Gamma) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \mathsf{SnapshotValid}(\Gamma, H_3)\right\}$$

$\texttt{else}$

$\texttt{rcuSynchronize}(q)$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \mathsf{DeallocBetween}(\Gamma, H_1, H_3) * \mathsf{FreeValid}(\Gamma) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} \\ \quad * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times (\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$$\left\{\begin{array}{l}\exists L_d, L'_d.\, \mathsf{RevokedUpTo}(\Gamma, H_3) * \mathsf{FreeValid}(\Gamma) * \mathsf{Stack}(q, L_d) * \square(\mathsf{NoDup}(L_d)) * \square(\mathsf{NoDup}(L'_d)) * \mathsf{DeadFrom}(L_d, L'_d, H_1, H_3) \\ \quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times (\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \mathsf{FreeValid}(\Gamma) * \mathsf{Stack}(q, L_d) * \mathsf{DeadFrom}(L_d, L'_d, H_1, H_3) \\ \quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times (\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1))}\end{array}\right\}$$

$$\left\{\begin{array}{l}\exists L_1, L_2, L'_1, L'_2.\, L_1 \cdot L_2 = L_d * L'_1 \cdot L'_2 = L'_d * |L_2| = |L'_2| \\ \quad * \mathsf{RevokedUpTo}(\Gamma, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \mathsf{DeadFrom}(L_2, L'_2, H_1, H_3) * \mathsf{FreeValid}(\Gamma) \\ \quad * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times ((\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1)) \setminus L'_1)} * \mathsf{Stack}(q + \texttt{del}, L_2)\end{array}\right\}$$

$\texttt{repeat}$

$$\left\{\begin{array}{l}\square(L_1 \cdot L_2 = L_d * L'_1 \cdot L'_2 = L'_d * |L_2| = |L'_2|) * \mathsf{RevokedUpTo}(\Gamma, H_3) * \mathsf{FreeValid}(\Gamma) * \mathsf{DeadFrom}(L_2, L'_2, H_1, H_3) \\ \quad * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times ((\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1)) \setminus L'_1)} * \mathsf{Stack}(q + \texttt{del}, L_2)\end{array}\right\}$$

$\texttt{let } p = \texttt{pop}(q + \texttt{del})$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \mathsf{FreeValid}(\Gamma) * \mathsf{DeadFrom}(L_2, L'_2, H_1, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} \\ \quad * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times ((\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1)) \setminus L'_1)} \\ \quad * ((p = 0 * L_2 = \texttt{nil} * \mathsf{Stack}(q + \texttt{del}, \texttt{nil})) \\ \qquad \vee (p \neq 0 * \exists P_2, P'_2, i'.\, L_2 = p \cdot P_2 * L'_2 = i' \cdot P'_2 * \mathsf{Stack}(q + \texttt{del}, P_2) \\ \qquad\quad * i' \in (\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1) \setminus L'_1)))\end{array}\right\}$$

$\texttt{if } p == 0 \texttt{ then } 1$

$\texttt{else}$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \mathsf{FreeValid}(\Gamma) * \mathsf{DeadFrom}(L_2, L'_2, H_1, H_3) \\ \quad * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times ((\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1)) \setminus L'_1)} \\ \quad * \mathsf{Stack}(q + \texttt{del}, P_2) * \square(L_2 = p \cdot P_2 * L'_2 = i' \cdot P'_2) * \square(i' \in (\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1) \setminus L'_1))\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \mathsf{FreeValid}(\Gamma) * \mathsf{DeadFrom}(P_2, P'_2, H_1, H_3) \\ \quad * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times ((\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1)) \setminus (L'_1 \cdot i'))} \\ \quad * \mathsf{Stack}(q + \texttt{del}, P_2) * p + \texttt{data} \hookrightarrow - * \exists j, S.\, \boxed{p + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, p, j)} * \boxed{j : \mathrm{Master}(S)}\end{array}\right\}$$

$\texttt{push}(q + \texttt{free}, p);$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \mathsf{FreeValid}(\Gamma) * \mathsf{DeadFrom}(P_2, P'_2, H_1, H_3) \\ \quad * \boxed{\Gamma.\mathsf{rxtok} : \{0, \ldots, N\} \times ((\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1)) \setminus (L'_1 \cdot i'))} \\ \quad * \mathsf{Stack}(q + \texttt{del}, P_2)\end{array}\right\}$$

0

`end`

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_3) * \mathsf{FreeValid}(\Gamma) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)} * \boxed{\Gamma.\mathsf{rxtok} : \{0,\dots,N\} \times (\mathsf{dead}(H_3) \setminus \mathsf{dead}(H_1))} \\ \quad * \mathsf{Stack}(q + \mathtt{del}, \mathtt{nil})\end{array}\right\}$$

$$\left\{\begin{array}{l}\exists H_1.\, H_1 \le H_3 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{FreeValid}(\Gamma) * \mathsf{DeallocBetween}(\Gamma, H_1, H_3) \\ \quad * \mathsf{SnapshotValid}(\Gamma, H_3) * \boxed{\Gamma.\mathsf{history} : \mathrm{Master}(H_3)}\end{array}\right\}$$

C.4.10 Verification of Writer $p + \mathtt{link}$ and $p + \mathtt{data}$ rules

$$\begin{array}{l}\{\mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L')\} \\ \quad [p + \mathtt{link}]_{\mathtt{at}} \\ \left\{\begin{array}{l}p'.\, \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L') * ((p' = 0 \wedge L' = \mathtt{nil}) \\ \quad \vee (p' \neq 0 \wedge \exists L'', v'.\, L' = (p', v') \cdot L''))\end{array}\right\}\end{array}$$

$$\begin{array}{l}\{\mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L') \wedge v \neq \mathsf{null}\} \\ \quad [p + \mathtt{data}]_{\mathtt{na}} \\ \{x.\, x = v \wedge \mathsf{WriterSafe}(q, L \cdot (p, v) \cdot L')\}\end{array}$$

These follow from the definition of TraceSpine. For the first triple, consider the case where L' is of the form $(p', v') \cdot L''$. Then the writer will have $\exists i, i', j, j', R, R', L$ such that $\boxed{p + \mathtt{link} : (i \cdot R, i' \cdot L) \mid \mathbf{LLP}(\Gamma, p, j)}$ and $\boxed{p' + \mathtt{link} : (i' \cdot R', -) \mid \mathbf{LLP}(\Gamma, p, j)}$ in addition to $\boxed{j : \mathrm{Master}_N(i \cdot R)}$ and $\boxed{j' : \mathrm{Master}_N(i' \cdot R')}$ with some master snapshot H such that $H_*(p) = i \cdot R$, $H_*(p') = i' \cdot R$, and $H(i) = i' \cdot -$. Now, when it reads $p + \mathtt{link}$, it knows that the state it sees must be $(i \cdot R', i' \cdot L)$ because neither component could be larger since that would require snapshots that are incompatible with the writer's master copies. Suppose the value read is l. There will be a snapshot of some trace H' in the protocol interpretation such that $H'_*(l) = i' \cdot -$. Hence, an action of the form $\mathtt{alloc}(l, i', -)$ must appear in H'. We must have that $H' \le H$ by the monoid composition rules, so this means this action also appears in H. But we already know that $\mathtt{alloc}(p', i', -)$ appears in H, and in a well-formed trace, actions of the form $\mathtt{alloc}(-, i', -)$ can appear at most once, we must have that $l = p'$. On the other hand, if $L' = \mathtt{nil}$, then TraceSpine guarantees that $p + \mathtt{link}$ must be exactly in a state where the second component is of the form $\mathsf{null} \cdot -$. But then the **LLP** protocol says that the value read must be 0.

For the second triple, since $v \neq \mathsf{null}$, it must be the case that L is non-empty, hence (p, v) is not the first element in the list in the TraceSpine predicate, which immediately guarantees that this predicate contains $p + \mathtt{data} \overset{N}{\hookrightarrow} v$.

C.4.11 Verification of `rcuNodeUpdate`

$$\begin{array}{l}\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L') * P(v_1')\} \\ \quad \mathtt{rcuNodeUpdate}(q, x, p, v_1') \\ \{x'.\, \mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x', v_1') \cdot L')\}\end{array}$$

This is one of the functions that does more than just swap around permissions via exchanges, so we take the time to give an intuitive sketch.

At some point the writer needs to introduce a new abstract location, which will be paired with the new node's `link` pointer. We will pick one from the set of abstract locations that are not mentioned anywhere in the master trace. Since the set of nodes mentioned in the master trace is finite this is always possible.

The SinglePtr property is important for the next step, which involves switching the old node to the dead state in the trace after we update the parent's pointer. We can only do this if we show that no node is pointing to the old node any longer. But by the SinglePtr property, the only node pointing it initially was the parent node, which we've now updated to point to the new node. Moreover, the new node we just added in does not point to it, because it points to the old node's child, which again by the SinglePtr cannot be the old node. So, the old node can be safely marked as dead.

Notice that it is only the writer that cares about the fact that there are no cycles in the list. The readers' correctness does not rely on this directly. In fact, it would be fine for the writer to make a cycle in the list, the problem is that it would need to be careful about how it then updated the list if it did, since a node could have more than one parent, so simply changing one of the parent's pointers would not be enough to make the node inaccessible.

$$\left\{\mathsf{WriterSafe}(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L') * \Box(P(v_1'))\right\}$$

$$\left\{\begin{array}{l}\exists \Gamma, H_1, H_2, H_3.\, \Gamma.q = q * H_1 \le H_2 \le H_1 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3)\end{array}\right\}$$

$$\left\{\begin{array}{l}\square(\Gamma.q = q) * \square(H_1 \le H_2 \le H_1) * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3)\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) * \exists i_p, i_x.\, H_{3*}(p) = i_p \cdot - * H_{3*}(x) = i_x \cdot - * H_3(i_p) = i_x \cdot -*\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) * \square(H_{3*}(p) = i_p \cdot - * H_{3*}(x) = i_x \cdot - * H_3(i_p) = i_x \cdot -*)\end{array}\right\}$$

$\texttt{let}\ c = [x + \texttt{link}]_{\texttt{at}}$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad * \exists i_c.\, \mathsf{hd}(H_3(i_x)) = i_c * ((c = 0 * L' = \texttt{nil}) \vee (c \neq 0 * \exists v_2, L''.\, L' = (c, v_2) \cdot L''))\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad * \square(\mathsf{hd}(H_3(i_x)) = i_c * ((c = 0 * L' = \texttt{nil} * i_c = \mathsf{null}) \vee (c \neq 0 * i_c \neq \mathsf{null} * \exists v_2, L''.\, L' = (c, v_2) \cdot L'' * H_{3*}(c) = i_c \cdot -)))\end{array}\right\}$$

$\texttt{let}\ x' = \texttt{rcuAlloc}(2)$ *`/* node = value, child pointer */`*

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad ((\exists S, j.\, \boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} * \boxed{j : \mathrm{Master}(S)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad ((\exists S, j.\, \boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} * \boxed{j : \mathrm{Master}(S)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data}))) \\ \quad * \exists i'_x.\, i'_x \notin \mathrm{dom}(H_3)\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad ((\exists S, j.\, \boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} * \boxed{j : \mathrm{Master}(S)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data}))) \\ \quad * \square(i'_x \notin \mathrm{dom}(H_3))\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad \exists S, j.\, \boxed{j : \mathrm{Master}(i'_x \cdot S)} * ((\boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad \boxed{j : \mathrm{Master}(i'_x \cdot S)} * ((\boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))\end{array}\right\}$$

$[x' + \texttt{data}]_{\texttt{na}} := v'_1;$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad \boxed{j : \mathrm{Master}(i'_x \cdot S)} * x' + \texttt{data} \hookrightarrow v'_1 * (\boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} \vee \mathsf{uninit}(x' + \texttt{link}))\end{array}\right\}$$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad \boxed{j : \mathrm{Master}(i'_x \cdot S)} * x' + \texttt{data} \hookrightarrow v'_1 * (\boxed{x' + \texttt{link} : (S, -) \mid \mathbf{LLP}(\Gamma, x', j)} \vee \mathsf{uninit}(x' + \texttt{link}))\end{array}\right\}$$

$[x' + \texttt{link}]_{\texttt{at}} := c;$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3 \cdot \mathtt{alloc}(x', i'_x, i_c)) \\ \quad \boxed{j : \mathrm{Master}(i'_x \cdot S)} * x' + \texttt{data} \hookrightarrow v'_1 * \boxed{x' + \texttt{link} : (i'_x \cdot S, i_c) \mid \mathbf{LLP}(\Gamma, x', j)}\end{array}\right\}$$

$[p + \texttt{link}]_{\texttt{at}} := x';$

$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x', v'_1) \cdot L', H_3 \cdot \mathtt{alloc}(x', i'_x, i_c) \cdot \mathtt{upd} i_p, i'_x \cdot \mathtt{del}(i_x)) \\ \quad * (\forall n < N.\, \mathsf{PermX}(\Gamma, x, n, i_x)) * \exists j'.\, \boxed{x + \texttt{link} : H_{3*}(x), H_3(i_x) \mid \mathbf{LLP}(\Gamma, x, j')} * \boxed{j' : \mathrm{Master}_N(H_{3*}(x))} * x + \texttt{data} \overset{N}{\hookrightarrow} -\end{array}\right\}$$

$\texttt{rcuDealloc}(q, x);$

$$\left\{\begin{array}{l}\exists H_1.\, H_1 \le (H_3 \cdot \mathtt{alloc}(x', i'_x, i_c) \cdot \mathtt{upd}(i_p, i'_x) \cdot \mathtt{del}(i_x)) * \mathsf{RevokedUpTo}(\Gamma, H_1) \\ \quad * \mathsf{DeallocBetween}(\Gamma, H_1, H_3 \cdot \mathtt{alloc}(x', i'_x, i_c) \cdot \mathtt{upd}(i_p, i'_x) \cdot \mathtt{del}(i_x)) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) + \cdot (x', v'_1) \cdot L', H_3 \cdot \mathtt{alloc}(x', i'_x, i_c) \cdot \mathtt{upd}(i_p, i'_x) \cdot \mathtt{del}(i_x))\end{array}\right\}$$

x'

$$\left\{x'.\, \mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot (x', v'_1) \cdot L')\right\}$$

C.4.12 Verification of `rcuNodeAppend`

$$\{\mathsf{WriterSafe}'(q, L \cdot (p, v_0)) * P(v_1')\}$$
$$\texttt{rcuNodeAppend}(q, p, v_1')$$
$$\{x'.\, \mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot (x, v_1'))\}$$

$\{\mathsf{WriterSafe}(q, L \cdot (p, v_0)) * \square(P(v_1'))\}$
$\{\exists \Gamma, H_1, H_2, H_3.\, \Gamma.q = q * H_1 \le H_2 \le H_1 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma)$
$\quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)\}$
$\{\square(\Gamma.q = q) * \square(H_1 \le H_2 \le H_1) * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma)$
$\quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma)$
$\quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3) * \exists i_p, i_x.\, H_{3*}(p) = i_p \cdot - * H_3(i_p) = \mathsf{null} \cdot -*\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma)$
$\quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3) * \square(H_{3*}(p) = i_p \cdot - * H_3(i_p) = \mathsf{null} \cdot -*)\}$
$\texttt{let}\ x' = \texttt{rcuAlloc}(2)$ *`/* node = value, child pointer */`*
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)$
$\quad ((\exists S, j.\, \boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} * \boxed{j : \mathrm{Master}(S)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)$
$\quad ((\exists S, j.\, \boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} * \boxed{j : \mathrm{Master}(S)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))$
$\quad * \exists i_x'.\, i_x' \notin \mathrm{dom}(H_3)\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)$
$\quad ((\exists S, j.\, \boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} * \boxed{j : \mathrm{Master}(S)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))$
$\quad * \square(i_x' \notin \mathrm{dom}(H_3))\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)$
$\quad \exists S, j.\, \boxed{j : \mathrm{Master}(i_x' \cdot S)} * ((\boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)$
$\quad \boxed{j : \mathrm{Master}(i_x' \cdot S)} * ((\boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} * x' + \texttt{data} \hookrightarrow -) \vee (\mathsf{uninit}(x' + \texttt{link}) * \mathsf{uninit}(x' + \texttt{data})))\}$
$[x' + \texttt{data}]_{\texttt{na}} := v_1';$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0), H_3)$
$\quad \boxed{j : \mathrm{Master}(i_x' \cdot S)} * x' + \texttt{data} \hookrightarrow v_1' * (\boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} \vee \mathsf{uninit}(x' + \texttt{link}))\}$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3)$
$\quad \boxed{j : \mathrm{Master}(i_x' \cdot S)} * x' + \texttt{data} \hookrightarrow v_1' * (\boxed{x' + \texttt{link} : (S, -)}\,\boxed{\mathbf{LLP}(\Gamma, x', j)} \vee \mathsf{uninit}(x' + \texttt{link}))\}$
$[x' + \texttt{link}]_{\texttt{at}} := 0;$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma)$
$\quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3 \cdot \texttt{alloc}(x', i_x', \mathsf{null}))$
$\quad \boxed{j : \mathrm{Master}(i_x' \cdot S)} * x' + \texttt{data} \hookrightarrow v_1' * \boxed{x' + \texttt{link} : (i_x' \cdot S, \mathsf{null})}\,\boxed{\mathbf{LLP}(\Gamma, x', j)}\}$
$[p + \texttt{link}]_{\texttt{at}} := x';$
$\{\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma)$
$\quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x', v_1'), H_3 \cdot \texttt{alloc}(x', i_x', \mathsf{null}) \cdot \mathsf{upd}(i_p, i_x'))\}$
x'
$\{x'.\, \mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot (x', v_1'))\}$

C.4.13 Verification of `rcuNodeDelete`

$$\{\mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L')\}$$
$$\texttt{rcuNodeDelete}(q, x, p)$$
$$\{\mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot L')\}$$

$$\left\{\mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot (x, v_1) \cdot L')\right\}$$
$$\left\{\begin{array}{l}\exists \Gamma, H_1, H_2, H_3.\, \Gamma.q = q * H_1 \le H_2 \le H_1 * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) \\ \quad * \mathsf{CurrentState}(\Gamma, \cdot(p, v_0) \cdot (x, v_1) \cdot L'), H_3)\end{array}\right\}$$
$$\left\{\begin{array}{l}\square(\Gamma.q = q) * \square(H_1 \le H_2 \le H_1) * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) \\ \quad * \mathsf{CurrentState}(\Gamma, \cdot(p, v_0) \cdot (x, v_1) \cdot L'), H_3)\end{array}\right\}$$
$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{CurrentState}(\Gamma, \cdot(p, v_0) \cdot (x, v_1) \cdot L'), H_3) \\ \quad * \exists i_p, i_x.\, H_{3*}(p) = i_p \cdot - * H_{3*}(x) = i_x \cdot - * H_3(i_p) = i_x \cdot -*\end{array}\right\}$$
$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) * \square(H_{3*}(p) = i_p \cdot - * H_{3*}(x) = i_x \cdot - * H_3(i_p) = i_x \cdot -*)\end{array}\right\}$$
$\texttt{let}\ c = [x + \texttt{link}]_{\texttt{at}}$
$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad * \exists i_c.\, \mathsf{hd}(H_3(i_x)) = i_c * ((c = 0 * L' = \texttt{nil}) \vee (c \ne 0 * \exists v_2, L''.\, L' = (c, v_2) \cdot L''))\end{array}\right\}$$
$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot (x, v_1) \cdot L', H_3) \\ \quad * \square(\mathsf{hd}(H_3(i_x)) = i_c * ((c = 0 * L' = \texttt{nil} * i_c = \mathsf{null}) \vee (c \ne 0 * i_c \ne \mathsf{null} * \exists v_2, L''.\, L' = (c, v_2) \cdot L'' * H_{3*}(c) = i_c \cdot -)))\end{array}\right\}$$
$[p]_{\texttt{at}} := c;$
$$\left\{\begin{array}{l}\mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_2) * \mathsf{FreeValid}(\Gamma) * \ \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot L', H_3 \cdot \texttt{upd} i_p, i_c \cdot \texttt{del}(i_x)) \\ \quad * (\forall n < N.\, \mathsf{PermX}(\Gamma, x, n, i_x)) * \exists j'.\, \boxed{x + \texttt{link} : H_{3*}(x), H_3(i_x) \mid \mathbf{LLP}(\Gamma, x, j')} * \boxed{\boxed{j' : \mathrm{Master}_N(H_{3*}(x))}}^{\text{dashed}} * x + \texttt{data} \overset{N}{\hookrightarrow} -\end{array}\right\}$$
$\texttt{rcuDealloc}(q, x);$
$$\left\{\begin{array}{l}\exists H_1.\, H_1 \le (H_3 \cdot \texttt{upd}(i_p, i_c) \cdot \texttt{del}(i_x)) * \mathsf{RevokedUpTo}(\Gamma, H_1) * \mathsf{DeallocBetween}(\Gamma, H_1, H_3 \cdot \texttt{upd}(i_p, i_c) \cdot \texttt{del}(i_x)) \\ \quad * \mathsf{CurrentState}(\Gamma, L \cdot (p, v_0) \cdot L', H_3 \cdot \texttt{upd}(i_p, i_c) \cdot \texttt{del}(i_x))\end{array}\right\}$$
$$\left\{\mathsf{WriterSafe}'(q, L \cdot (p, v_0) \cdot L')\right\}$$